INTEGRATED CIRCUITS

DATA HANDBOOK

Advanced CMOS Logic
ACL
Supplement to IC07

BOOK IC07 1991

Philips Components

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ADVANCED CMOS LOGIC ACL SUPPLEMENT

Preface

ACL Supplement

Since the publication of the ACL book in September of 1989, some changes, deletions, and upgrades have been made to our product line. This supplement contains such changes and is meant to supercede any specifications previously published in the 1989 edition.

We would like to thank you for your continued interest in our ACL product line. Utilizing a 1 micron CMOS process, Philips Components–Signetics' ACL is one of the lowest power-delay product families in the market today.

Standard Products Group

Product Status

ACL Supplement

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Section 1

ACL Products

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Introduction

INTRODUCTION

There is little doubt that CMOS is closing in on bipolar technology as the mainstay of integrated commodity logic. Advancing technology is rapidly eliminating the old trade-offs between speed and power dissipation (see Figure 1), and problems peculiar to CMOS such as latch-up and ESD sensitivity have already been solved. However, until now, CMOS logic ICs have been unable to match the high speed and the high current output of TTL technologies which is essential for operation in the bus or transmission line environment of the fastest logic systems.

The introduction of the Advanced CMOS Logic (ACL) family of ICs removes this hurdle. Signetics fabricates ACL in a 1-micron twin-well CMOS process with recessed local oxidation and a titanium disilicide layer on the gate, source and drain areas to reduce the contact and interconnect resistance. This, together with oxidation of the gate sidewalls for reduced capacitance, leads to increased drive and speed that equals that of the fastest bipolar TTL logic. With an average propagation delay of 5ns (150MHz operation) and 24mA sink/source capability, ACL supplements the HE4000B and HCMOC IC ranges to allow designers to implement the outstanding CMOS benefits of wide and symmetrical noise margins, high reliability, and reduced power dissipation across the whole speed spectrum of logic circuitry.

The inevitable fast edges associated with the exceptionally high speed of ACL required one final hurdle to be removed: the problem, which also exists for fast-switching bipolar logic, can reduce system noise margins, cause loss of stored data and reduce system speed. We have solved it for ACL by discarding the traditional corner supply pinning arrangement and simultaneously adopting a flowthrough architecture wherein the supply pins are at the center of each side of the package (where the internal inductance is minimum), all the input pins are on one side, all the output pins are on the other, and control pins are at the corners. Although this solution means that ACL is not pin-compatible with the comparable TTL and HCMOS functions, as an engineering-driven company, we felt that the considerations of improving system reliability, simplifying pcb design and reducing board area should take precedence.

All types within our ACL family have outputs that are both CMOS and TTL-compatible and are available for operating temperature ranges of -40°C to +85°C (commercial/industrial: 74AC/ACT prefix) or -55°C to +125°C (military: 54AC/ACT prefix). They come in two versions:

- Fully buffered 54/74AC types with CMOS-compatible input switching levels (typically $V_{CC}/2$) and a supply voltage range of 3V to 5.5V for all-CMOS systems
- Fully buffered 54/74ACT types with TTL-compatible input switching levels (typically 1.5V) and a supply voltage range of 5V±10% for interfacing with TTL systems

Since the low power dissipation of our ACL ICs makes them ideal for circuitry on densely packed boards in small enclosures, we didn't overlook the need to make them compatible with surface mounting technology which is being increasingly used for automated assembly of electronic equipment to achieve significant reduction of its size and weight. Production quantities of *all* our ACL ICs are available in DIP packages and in SO (small outline) packages. The dimensions of the latter were originally developed by us and now form the basis of JEDEC standard publication 95 (also published in IEC standard document 191-2, family A76).

ACL ICs are completely latch-up free and have complete protection against electrostatic discharge (ESD) at their inputs.

ACL IN A NUTSHELL

ACL has all the well-known attributes of our HCMOS family combined with faster operation and increased drive capability. Here are 14 reasons why Signetics is head and shoulders above the rest:

- A comprehensive type range from simple gates to shift registers and counters
- All types available in 74AC versions (CMOS input levels) and 74ACT versions (TTL input levels)
- All types available in SO (small outline) packages as well as in DIP, so you can use surface-mount techniques to increase pcb packing density. The 14 and 16-pin SO packages are the narrower 150mil (3.8mm) versions and are available on 16mm tape on 13 inch diameters reels (2500 ICs). The 16, 20, 24 and 28-pin SO packages are 300mil (7.6mm) wide and are available on 24mm tape with 1000 ICs on a 13 inch reel. The body width of all the DIP packages (14 to 28 pins) is 300mil (7.6mm).
- Completely latch-up free and fully ESD protected up to ±2kV (human body model) at all inputs and outputs.
- Low power dissipation. Typical quiescent current per package is only a few nanoamps for gates, flip-flops and MSI. Typical counter operating current with a 5V supply is 250µA at 1MHz and increases linearly with frequency.
- 24mA sink/source current. For incident wave switching 74AC/ACT types can provide ±75mA (for driving a 50Ω load).
- ACL input current is only 1µA in the High or Low state. This is essentially zero compared with the input current of TTL technologies. The fan-out to other CMOS ICs is therefore only limited by load capacitance considerations and not by DC loads.

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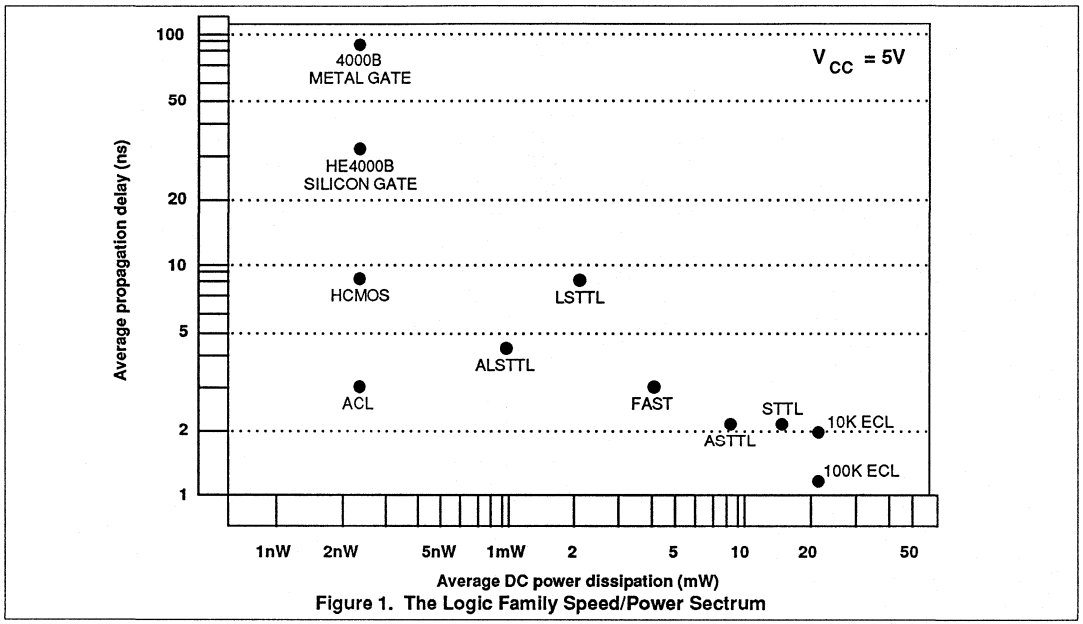

Figure 1. The Logic Family Speed/Power Sectrum

- More than three times the noise immunity of TTL. Input switching levels are between 30% and 70% of V_{CC} for 74AC types and between 0.8V and 2V for 74ACT types. The output swing for all ACL ICs is from 0.1V to V_{CC}-0.1V with a load of 50μA (fifty ACL inputs), and from 0.5V to V_{CC}-0.8V with a load of ±24mA.
- The input switching threshold level is subject to a variation of only ±60mV over the entire temperature range, much less than the ±300mV specified for advanced TTL families.
- Wide supply voltage range. AC versions are specified with a supply from 3V to 5.5V (the internal logic state is maintained down to 2V). Battery back-up is no problem and automotive applications are possible. TTl-compatible ACT versions are specified with a supply of 5V ± 10%.
- With a 5V supply, average propagation delay for a gate is 5ns for either High-to-Low or Low-to-High transitions into a capacitive load of 50pF. On-chip propagation delay for gates is only 0.5ns. Typical operating frequency is up to 150MHz at 25°C and f_{MAX} is simply specified with a 50% duty factor.
- Outputs have edge control circuits to reduce the effective dv/dt, thereby further reducing switching noise. The output buffers are standardized to allow symmetrical output current sourcing and sinking for equal output rise and fall times. This results in simplified design combined with optimum speed and AC performance.
- Center supply pins and flowthrough architecture to minimize ground and supply rail glitches during simultaneous switching of outputs, and to simplify board layout.
- All ACL critical inputs have a new patented dynamic hysteresis to make them less susceptible to slow input edges. (A critical input is considered an input which controls more than one output.)
- Extensive customer support is available.
- Signetics ACL ICs are alternate-source by TI.

A CLOSER LOOK AT ACL

Supply Voltage

ACL circuits with the type number prefix 74AC operate from a supply voltage range of 3V to 5.5V which meets the new industry JEDEC standard No. 8 which specifies 3.3V ±0.3V for regulated power supply systems. The internal logic of 74AC circuits will, however, maintain its state with a supply voltage as low as 2V. This facilitates the use of a lithium battery as a back-up supply. ACL circuits with the type number prefix 74ACT operate from a supply voltage of 5V ±10% which is consistent with the supply voltage for the TTL logic circuits with which they are intended to interface.

Power Dissipation

One of the most important requirements for any logic system is low power dissipation because it minimizes system cost, allows higher packing density, and results in improved reliability because of lower operating temperature.

The typical quiescent power dissipation of an ACL gate (2.5nW) is more than six orders of magnitude less than that of bipolar TTL functions. This is because,

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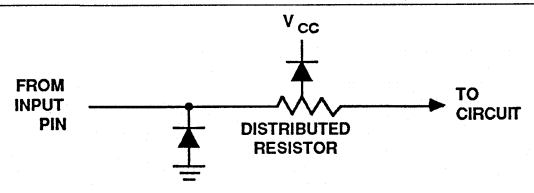
unlike TTL circuits, CMOS circuits dissipate only negligible power due to leakage currents when they are not switching. The maximum quiescent current per ACL package for SSI (40μA) is less than 1% of that of an equivalent TTL package with 50% of the gates in the High state. The typical dynamic power dissipation of ACL gates is also very low. With 50pF load and a 5V supply, it is 0.18mW at 100kHz rising to only 18mW at 10MHz, two-thirds of which is dissipated in the load capacitance. This is considerably lower than that of the fastest TTL circuits, particularly at lower frequencies where their high quiescent current predominates over their dynamic current.

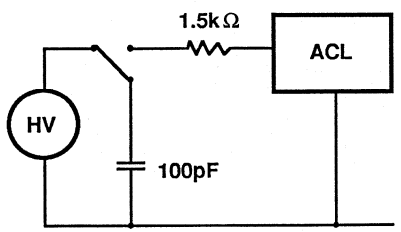
The power cross-over frequency where ACL and TTL dissipate the same power is about 10MHz for a gate, and more than 20MHz for a flip-flop. However, in a practical logic system, only a few of the logic elements operate at the maximum clock frequency, so the average operating frequency is much lower, giving ACL ICs an even greater advantage over advanced TTL. In a more complex system comprising a divider chain of six flip-flops, the power cross-over frequency no longer exists. At 30MHz, ACL still dissipates only one sixth of the equivalent advanced TTL dissipation. If the divider chain is lengthened, or the system complexity increased, the power saving increases even more.

Propagation Delay

The on-chip propagation for a single ACL gate is only 0.5ns. For an entire ACL package with a 50pF load, it is 5ns average for High-to-Low or Low-to-High transitions. Moreover, propagation delay is specified over the entire operating temperature range and at two system supply voltages (3.3V ± 0.3V and 5V ± 0.5V). For user convenience, we also specify the minimum propagation delay. The specified limits are comparable to those for the most advanced TTL logic. The AC characteristics of ACL are improved by standardized output buffers which allow equal rise and fall times. The typical switching frequency limit for ACL is 150MHz at 25°C and is specified with a 50% duty factor so you don't have to tweak the pulse widths as you do with TTL. Due to the high drive current capability of the low impedance ACL outputs, propagation delay variation as a function of load capacitance is much less than that of most other logic ICs.



(a) ACL Input Protection Network



(b) 'Human Body Model' Test Arrangement

Figure 2. The Inputs of ACL ICs Are Fully Protected Against ESD.

Noise Immunity

The input switching levels for 74AC ICs are always between 30% and 70% of V_{CC}. Output swing is from 0.1V to V_{CC}-0.1V with a load of 50μA (50 CMOS inputs). For 74AC circuits driving 50 CMOS inputs, the low- and high-level noise immunity with a 4.5V supply is, therefor, 28% of V_{CC}. It is even greater for a higher supply voltage, 74ACT ICs match the Low-level noise immunity of TTL at higher operating temperatures (up to 85°C) and exceed it at 70°C. The High-level noise immunity is three times that of TTL. ACL ICs are, therefore, ideally suited for use in electrically noisy environments such as those encountered in industry, telephony and automotive applications.

Drive Capability

Although the ACL family has the low input current which is a characteristic of CMOS circuits, it is capable of providing output current of up to 24mA without sacrifice of noise immunity or switching speed. Moreover, unlike the fastest TTL circuits, all ACL ICs have standardized output buffers which allow symmetrical output current sinking and sourcing to obtain equal rise and fall times. This simplifies design and results in optimum speed and AC performance.

The drive current specified for ACL is valid over the entire operating temperature range and, since the input current for ACL circuits is only 1μA in the High or Low state, the fan-out when driving other CMOS circuits is only limited by load capacitance considerations and not by the available drive power. However, in the fastest logic systems, ACL will probably be working in a transmission line environment where its low output resistance (20Ω max.) is of particular significance for reducing a system's susceptibility to crosstalk and induced noise, and for guaranteeing incident wave switching to optimize system speed. For example, to guarantee incident wave switching over the commercial temperature range, the sink/source capability of ACL is 75mA at V_O=1.65V which allows terminated lines with a characteristic impedance down to 50Ω to be driven at the maximum supply voltage.

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ESD Protection

The ACL input network shown in Figure 2(a) incorporates reverse-biased diodes between the positive rail, input pins and ground in order to clamp the input voltage to provide ESD protection and limit the amplitude of any ringing. These diodes have typical forward voltage drops of 0.9V and reverse breakdown voltages of 18V. ACL inputs can withstand ESD of greater than ±2kV from the 'human body model' (1.5k Ω, 100pF, 13ns pulse rise time) shown in Figure 2(b). This meets MIL-STD-883B, Method 3015.

Large inherent diodes formed by the drain surfaces of ACL output transistors provide protection and allow discharges up to 2kV to be sustained without damage to outputs.

ACL is Latch-up Free

Latch-up can be reduced by the use of extensive guard rings, but at the expense of increased chip area. In our ACL family, we've completely eliminated latch-up by growing the high-resistivity p^- epitaxial layer on a very low-resistivity p^+ layer and thereby prevents parasitic bipolar transistors from being forward biased. This, plus proprietary layout rules and process parameters that even further reduce the gain of the parasitic bipolar transistors, means that our ACL ICs are completely latch-up free.

We've subjected our ACL ICs to latch-up tests with ratings far exceeding those specified by JEDEC. In no case did latch-up occur. For example, input/outputs can withstand currents as high as 100mA DC or 450mA pulsed. V_{CC} breakdown for ACL ICs doesn't occur until a supply current of 6.8mA; this requires a supply voltage of more than 21V. After breakdown, the supply voltage always snaps back to a level far greater than the maximum operating supply voltage. So, latch-up will not occur in the event of severe supply over voltage.

74ACT - FOR INTERFACING WITH TTL

Since the entire type range of ACL ICs is also available in 74ACT versions, it is easy to drive ACL from ALS-TTL, AS-TTL or FAST-TTL outputs without using power consuming pull-up resistors at the bipolar logic outputs to maintain adequate noise margins.

All the advantages previously described for 74AC ICs naturally also apply to the 74ACT versions. The only differences are that the propagation delay is slightly longer and the nominal supply voltage and the input structure of the 74ACT types have been modified to match TTL characteristics. The modified input structure not only adapts to TTL input switching levels, but also reduces power consumption when a minimum TTL High output level of 2.4V is applied to a 74ACT input.

For TTL compatibility, the supply voltages for 74ACT ICs is 5V ±10%. Unlike 74AC ICs which have an input switching threshold of 50% of V_{CC}, the input switching threshold of 74ACT types is 1.5V and the inputs switch between the same levels as TTL (V_{ILmax}=0.8V, V_{IHmin}=2V). The temperature sensitivity of the input switching threshold, however, is only ±60mV over the entire temperature range, so the noise margins also remain very stable over the temperature range. With a 4.5V supply and an output current of 50µA (50 ACL inputs), a 74ACT output swings between 0.1V and V_{CC}-0.1V. With the maximum output current of 24mA, it swings between 0.5V and V_{CC}-0.8V. So, for a 74ACT IC with a 4.5V supply driving fifty ACL inputs, the noise margins are 53% of V_{CC} (High) and 15.5% of V_{CC} (Low). For a similar LSTTL IC, they would be only 15% of V_{CC}(High and 8% of V_{CC} (Low). Even when a 74ACT IC

SAFE DRIVING-INTERFACE REQUIREMENTS

Safe driving-interface requirements		TO					
		HC/AC 5V supply	HCT/ACT 5V supply	HE4000B 5V supply	HE4000B 6-15 V supply	TTL* 5V supply	ECL 10K
FROM	HC/AC 5V supply	direct	direct	direct	4104	direct	10124
	HCT/ACT 5V supply	direct	direct	direct	4104	direct	10124
	HE4000B 5V supply	direct	direct	direct	4104	direct	10124
	HE4000B 6-15V supply	4049 or 4050	4049 or 4050	4049 or 4050	direct	4049 or 4050	transistor
	TTL* 5V supply	pull-up resistor	direct	pull-up resistor	4104	direct	10124
	ECL 10K	10125	10125	10125	transistor	10124	direct

* Includes LS, S, STD, FAST, ALS and AS

NOTES:
direct = without interface components
4104 = Low-to-High level shifters from the HE4000B family
10124 = TTL to ECL translator from the ECL 10K and 100K families
10125 = ECL to TTL translator from the ECL 10K and 100K families
4049/4050 = High-to-Low level shifters from the HE4000B family

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is delivering 24mA, the noise margins are 42% of V_{CC} (High) and 6.6% of V_{CC} (Low).

ADVANCED TECHNOLOGY MAKES IT POSSIBLE

The 10-mask ACL construction is a result of our continuing development program to enhance the proven polycrystalline silicon (polysilicon) gate CMOS process. It incorporates several technological innovations for increasing packing density, speed, and reliability.

The twin-well p^-/n^- structure and double-layer metal interconnects allow a high packing density which will also facilitate development of future MSI/LSI circuitry.

Three main features contribute to the exceptionally high speed of ACL. Firstly, the effective length of the transistor gate is only 1µm, resulting in an on-chip propagation delay of only 0.5ns. Secondly, there is a self-aligning titanium disilicide (salicide) layer on the source gate and drain to reduce series resistance and to reduce contact resistance between the 2-layer metal interconnects and the junctions. Thirdly, oxidation of the sidewalls of the gate minimizes the gate/source and gate/drain capacitances.

Reliability is assured by using copper-doped aluminum on tungsten interconnects to achieve high resistance to electromigration. A very thin titanium layer below the tungsten promotes adhesion to the underlying oxide. Furthermore, a p^- epitaxial layer on a low-resistivity p^+ substrate results in a high degree of latch-up immunity.

NEW PINOUTS FOR ACL ADD RELIABILITY AND SIMPLIFY DESIGN

The fast rise and fall times associated with high speed logic can lead to noise problems when one or more outputs of an IC switch from one logic state to another. As shown in Figure 3 this discharges the load capacitances through the internal supply pin inductance, thereby causing a transient that lifts up the on-chip ground and reduces the effective supply voltage to the chip. The problems are particularly severe in CMOS logic in which the outputs can switch almost from one supply rail to the other. Referred to as simultaneous switching noise, the transient appears on any unswitched output(s) of the switching IC and has a peak amplitude directly proportional to the number of outputs simultaneously switched and to the internal inductance associated with the IC supply connections. This lifting up of the GND and consequent reduction of V_{CC} levels degrades system reliability by reducing noise margins, reducing speed, causing loss of stored data and causing false switching.

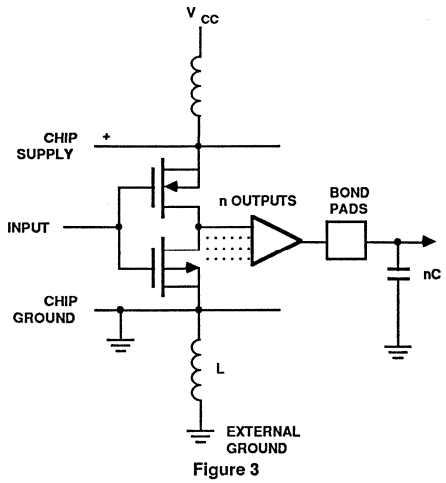


Figure 3

It is a common misconception that supply decoupling capacitors located adjacent to each IC will eliminate simultaneous output switching transients. The output capacitance discharge noise is related to the absolute inductance of the supply connection between the chip in the IC and the external supply groundplane. Since multilayer boards provide excellent supply and groundplanes, improvement can only be achieved by manufacturers taking measures to reduce the supply lead inductances within the IC. Supply line decoupling should be similar to that used for TTL systems operating at comparable speed.

In the early days of integrated logic, IC manufacturers were forced to position the supply pins at diagonally opposite corners of the package because of layout restrictions imposed by single-sided print-boards which were in universal use at that time. However, in today's world of double-sided and multilayer print-boards and much faster logic, placing the supply pins at diagonally opposite corners of the package where the long bonding wires and lead frame segments have the maximum inductance can no longer be considered to

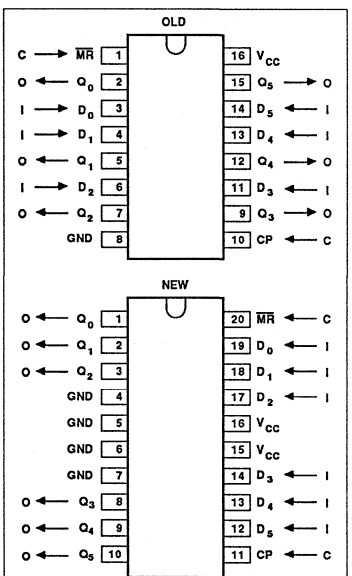


Figure 4 Flow-through Architecture of 74AC11174.

Introduction

be good engineering practice because it's the worst possible positioning from the point of view of simultaneous switching noise. So, for our ACL ICs, we've decided that optimum reliability is far more important than pin compatibility with TTL, and we've relocated the GND and V_{CC} pins; 16-pin ICs with 3 or 4 outputs have two GND pins and two V_{CC} pins; 20, 24 and 28-pin ICs with 3 or more outputs have four GND pins and two V_{CC} pins.

Tests performed on our octal ACL ICs with the new pinning reveal that, when seven outputs are simultaneously switched from High to Low, the amplitude of simultaneous switching noise stays well below the Low input switching level and is only about 35% of that for an IC with corner GND and V_{CC} pins.

We've also rationalized the positioning of the I/O and control pinning of ACL ICs as shown in Figure 4. All the inputs surround the V_{CC} pin(s) on the side of the package with the highest pin numbers, and all the outputs surround the GND pin(s) on the other side of the package. The control pins are strategically placed at the corners of the package. This ACL flow-through architecture, which is used for all ACL ICs in both DIP and SO packages, reduces the total inductance of outputs (bonding wire plus lead frame and output pin) between the chip and the pcb tracks. It also facilitates positioning of decoupling components, simplifies pcb design and fault-finding, and decreases the area of pcb required.

Alphanumeric Index

ACL Products

Functional Index

ACL Products

ACL 74AC/ACT11XXX FAMILY

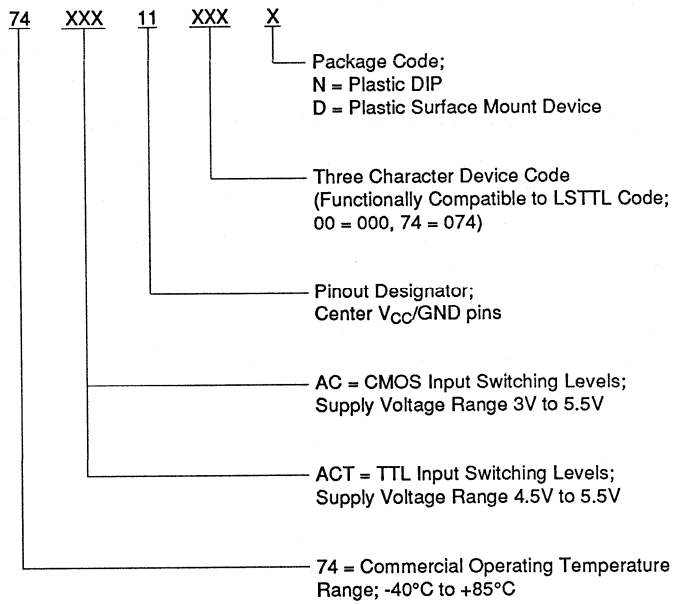
Type numbers have a suffix which signifies the type of package:
N = Plastic DIP; D = Plastic Surface Mount Device

Functional Index

Ordering Information

ACL Products

TYPE NUMBER DESIGNATIONS



Section 2
Family Characteristics

ACL Products

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Family Specifications

ACL Products

GENERAL
These family specifications cover the common electrical ratings and characteristics of the entire 74AC/ACT11XXX family, unless otherwise specified in the individual device data sheet.

INTRODUCTION
The 74AC/ACT11XXX 1μm CMOS Logic family combines the low power advantages of CMOS with the high speed and drive capability of FAST.

The basic family of devices designated as 74AC11XXX will operate at CMOS input logic levels for high noise immunity, negligible quiescent supply and input current. It is operated from a power supply of 3 to 5.5V.

A subset of the family designated as 74ACT11XXX with the same features and functions as the "AC-types" will operate at standard TTL power supply voltage (5V±10%) and logic input levels (0.8 to 2.0V).

HANDLING MOS DEVICES
Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations.

However, to be totally safe, it is desirable to take handling precautions into account.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±(n x 25)	mA
	DC ground current		±(n x 25)	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Family Specifications

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11XXX				74ACT11XXX				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off–state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.5		±0.5		5.5	μA
I_{CC}	Quiescent supply current, for SSI	V_I = V_{CC} or GND, I_O = 0mA		5.5		4.0		40		4.0		40	μA
	Quiescent supply current, for MSI	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

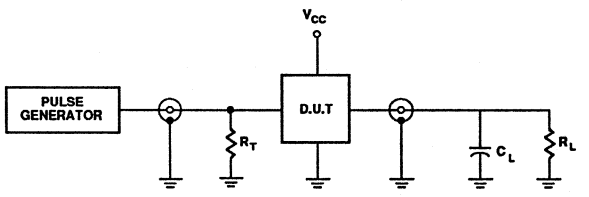
Family Specifications

RECOMMENDED OPERATING CONDITIONS

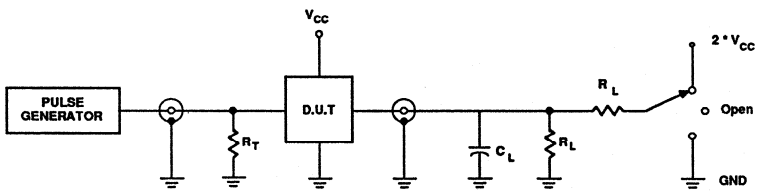
SYMBOL	PARAMETER							UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

TEST CIRCUIT



Test Circuit



Test Circuit for 3-State Devices

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Data Sheet Specification Guide

ACL Products

INTRODUCTION

The 74ACL data sheets have been designed for ease-of-use. A minimum of cross-referencing for more information is needed.

TYPICAL PROPAGATION DELAY AND FREQUENCY

The typical propagation delays listed at the top of the data sheets are the average of t_{PLH} and t_{PHL} for a typical data path through the device with a 50pF load.

For clocked devices, the maximum frequency of operation is also given. The typical operating frequency is the maximum device operating frequency with a 50% duty factor and no constraints on t_R and t_F.

LOGIC SYMBOLS

Two logic symbols are given for each device - the conventional one (Logic Symbol) which explicitly shows the internal logic (except for complex logic) and the IEEE/IEC Logic Symbol.

The IEEE/IEC has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic current to each output without explicitly showing the internal logic.

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table lists the maximum limits to which the device can be subjected without damage. This does not imply that the device will function at these extreme conditions, only that, when these conditions are removed and the device operated within the Recommended Operating Conditions, it will still be functional and its useful life will not have been shortened.

RECOMMENDED OPERATING CONDITIONS

The "Recommended Operating Conditions" table lists the operating ambient temperature and the conditions under which the limits in the "DC Characteristics" and "AC Characteristics" table will be met. The table should not be seen as a set of limits guaranteed by the manufacturer, but as the conditions used to test the devices and guarantee that they will then meet the limits in the DC and AC Characteristics tables.

TEST CIRCUITS

Good high-frequency wiring practices should be used in test circuits. Capacitor leads should be as short as possible to minimize ripples on the output waveform transitions and undershoot. Generous ground metal (preferably a ground plate) should be used for the same reasons. A V_{CC} decoupling capacitor should be provided at the test socket, also with short leads. Input signals should have rise and fall times of 3ns, a signal swing of 0V to V_{CC} for 74AC and 0V to 3V for 74ACT; a 5MHz square wave is recommended for most propagation delay tests. The repetition rate must be increased for testing f_{MAX}. Two pulse generators are usually required for testing such parameters as setup time, hold time and removal time. f_{MAX} is also tested with 3ns input rise and fall times, with a 50% duty factor, but for typical f_{MAX} as high as 150MHz, there are no constraints on rise and fall times.

DC CHARACTERISTICS

The "DC Characteristics" table reflects the DC limits used during testing. The values published are guaranteed.

The threshold values of V_{IH} and V_{IL} are applied to the inputs, the output voltages will be those published in the "DC Characteristics" table. There is a tendency, by some, to use the published V_{IH} and V_{IL} thresholds to test a device for functionality in a "function-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment with cables up to 1 meter. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, in the order of milliseconds, so that there is no noise at the inputs when the outputs are measured. But in functionality testing, the outputs are measured much faster, so there can be noise on the inputs, before the device has assumed its final and correct output state. Thus, never use V_{IH} and V_{IL} to test the functionality of any ACL device type; instead, use input voltages of V_{CC} (for the High state) and 0V (for the Low state). In no way does this imply that the devices are noise-sensitive in the final system.

In the data sheets, it may appear strange that the typical V_{IL} is higher than the maximum V_{IL}. However, this is because V_{ILMAX} is the maximum V_{IL} (guaranteed) for all devices that will be recognized as a logic Low. However, typically a higher V_{IL} will also be recognized as a logic Low. Conversely, the typical V_{IH} is lower than its minimum guaranteed level.

The quiescent supply current I_{CC} is the leakage current of all the reversed-biased diodes and the OFF-state MOS transistors.

AC CHARACTERISTICS

The "AC Characteristics" table lists the guaranteed limits when a device is tested under the conditions given in the AC Test Circuits and Waveform section.

Definitions of Symbols

ACL Products

DEFINITIONS OF SYMBOLS AND TERMS USED IN ACL DATA SHEETS

Current

Positive current is defined as conventional current flow into a device.

Negative current is defined as conventional current flow out of a device.

I_{CC} Quiescent power supply current; the current flowing into the V_{CC} supply terminal.

ΔI_{CC} Additional quiescent supply current per input pin at a specified input voltage and V_{CC}.

I_{GND} Quiescent power supply current; the current flowing into the GND terminal.

I_I Input leakage current; the current flowing into a device at a specified input voltage and V_{CC}.

I_{IK} Input diode current; the current flowing into a device at a specified input voltage.

I_{IO} Input/output source or sink current; the current flowing into a device at a specified input/output voltage.

I_O Output source or sink current; the current flowing into a device at a specified output voltage.

I_{OK} Output diode current; the current flowing into a device at a specified output voltage.

I_{OZ} OFF-state output current; the leakage current flowing into the output of a 3-State device in the OFF-state, when the output is connected to V_{CC} or GND.

Voltages

All voltages are referenced to GND (ground), which is typically 0V.

GND Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.

V_{CC} Supply voltage; the most positive potential on the device.

V_{EE} Supply voltage; one of two (GND and V_{EE}) negative power supplies.

V_H Hysteresis voltage; difference between the trigger levels when applying a positive and a negative-going input signal.

V_{IH} High-level input voltage; the range of input voltages that represents a logic High-level in the system.

V_{IL} Low-level input voltage; the range of input voltages that represents a logic Low-level in the system.

V_{OH} High-level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a High-level at the output.

V_{OL} Low-level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a Low-level at the output.

V_{T+} Trigger threshold voltage; positive-going signal.

V_{T-} Trigger threshold voltage; negative-going signal.

Capacitances

C_I Input capacitance; the capacitance measured at a terminal connected to an input of a device.

$C_{I/O}$ Input/Output capacitance; the capacitance measured at a terminal connected to an I/O-pin (e.g. a transceiver).

C_L Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.

C_{PD} Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function when no extra load is provided to the device.

AC Switching Parameters

f_I Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate High and Low for data input or using the toggle mode, whichever is applicable.

f_O Output frequency; each output.

f_{MAX} Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10% V_{CC} to 90% V_{CC} in accordance with device function table.

t_H Hold time; the interval immediately following the active transition of the timing pulse

Definitions of Symbols

(usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_R, t_F Clock input rise and fall times; 10% and 90% values.

t_{PHL} Propagation delay; the time between the specified reference points, normally the 50% points for 74AC devices on the input and output waveforms and the 1.5V points for the 74ACT devices, with the output changing from the defined High-level to the defined Low-level.

t_{PLH} Propagation delay; the time between the specified reference points, normally the 50% points for 74AC devices on the input and output waveforms and the 1.5V point for the 74ACT devices, with the output changing from the defined Low-level to the defined High-level.

t_{PHZ} 3-State output disable time; the time between the specified reference points, normally the 50% points for the 74AC devices and the 1.5V points for the 74ACT devices on the output enable input voltage waveform and a point representing 20% of the output swing on the output voltage waveform of a 3-State device, with the output changing from a High-level (V_{OH}) to a high-impedance OFF-state (Z).

t_{PLZ} 3-State output disable time; the time between the specified reference points, normally the 50% points for the 74AC devices and the 1.5V points for the 74ACT devices on the output enable input voltage waveform and a point representing 20% of the output swing on the output voltage waveform of a 3-State device, with the output changing from a Low-level (V_{OL}) to a high-impedance OFF-state (Z).

t_{PZH} 3-State output enable time; the time between the specified reference points, normally the 50% points for the 74AC devices and 1.5V points for the 74ACT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-State device, with the output changing from a high-impedance OFF-state (Z) to a High-level (V_{OH}).

t_{PZL} 3-State output enable time; the time between the specified reference points, normally the 50% points for the 74AC devices and the 1.5V points for the 74ACT devices on the output enable input voltage waveform and the 50% point on the output voltage waveform of a 3-State device with the output changing from a high-impedance OFF-state (Z) to a Low-level (V_{OL}).

t_{REC} Recovery time; the time between the end of and overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at the 50% points for 74AC devices and the 1.5V points for the 74ACT devices on both input voltage waveforms.

t_S Setup time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval data to be recognized must be maintained at the input to ensure their recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{THL} Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from High-to-Low.

t_{TLH} Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from Low-to-High.

t_W Pulse width; the time between the 50% amplitude points on the leading and trailing edges of a pulse for 74AC devices and at the 1.5V points for 74ACT devices.

Section 3
Data Sheets

ACL Products

INDEX

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

AC11013: Product Specification
ACT11013: Objective Specification
Dual 4-input NAND Schmitt-trigger

FEATURES

- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: SSI

DESCRIPTION

The 74AC/ACT11013 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11013 provides two separate 4-input NAND gate functions which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A, B, C, D to $\overline{Y}$	C_L = 50pF	4.3	8.0	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	29	32	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

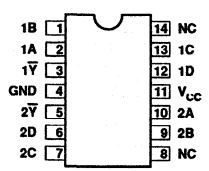
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

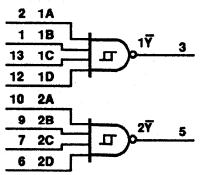
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11013N 74ACT11013N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11013D 74ACT11013D

PIN CONFIGURATION

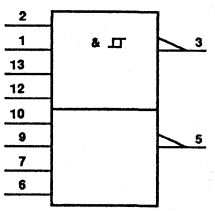
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Dual 4-input NAND Schmitt-trigger 74AC/ACT11013

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 10	1A - 2A	Data inputs
1, 9	1B - 2B	Data inputs
13, 7	1C - 2C	Data inputs
12, 6	1D - 2D	Data inputs
3, 5	$1\overline{Y}$ - $2\overline{Y}$	Data outputs
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	$n\overline{Y}$
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11013			74ACT11013			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	0		100	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Dual 4-input NAND Schmitt-trigger 74AC/ACT11013

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11013				74ACT11013				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{T+}	Positive-going threshold			3.0		2.2		2.2					V
				4.5		3.2		3.2		2.0		2.0	
				5.5		3.9		3.9		2.0		2.0	
V_{T-}	Negative-going threshold			3.0	0.5		0.5						V
				4.5	0.9		0.9			0.8		0.8	
				5.5	1.1		1.1			0.8		0.8	
ΔV_T	Hysteresis (V_{T+} - V_{T-})			3.0	0.3	1.2	0.3	1.2					V
				4.5	0.4	1.4	0.4	1.4	0.4	1.2	0.4	1.2	
				5.5	0.5	1.6	0.5	1.6	0.4	1.2	0.4	1.2	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		3.6		0.44					
			I_{OL} = 24mA	4.5		3.6		0.44		3.6		0.44	
				5.5		3.6		0.44		3.6		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±0.1		±0.1		±0.1	µA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		4.0		4.0		4.0		4.0	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11013					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	2.5 2.3	6.4 6.5	8.7 8.7	2.5 2.3	9.7 9.9	ns

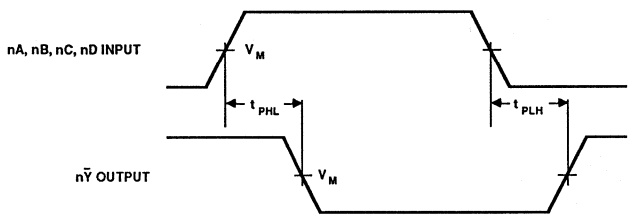
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11013					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	2.0 2.0	4.2 4.4	6.4 6.9	2.0 2.0	7.1 7.8	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11013					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB, nC, nD to n$\overline{Y}$	1	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (nA, nB, nC, nD) to Output (n$\overline{Y}$) Propagation Delays

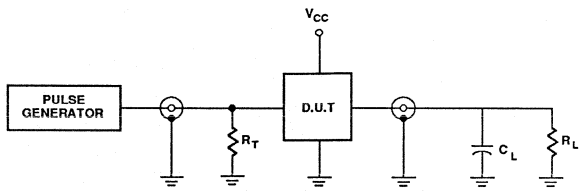
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

Dual 4-input NAND Schmitt-trigger

74AC/ACT11013

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

AC11014: Product Specification
ACT11014: Objective Specification

FEATURES

- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: SSI

DESCRIPTION

The 74AC/ACT11014 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11014 provides six separate inverters which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, to $\overline{Y}$	C_L = 50pF	3.6	8.5	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	27	36	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

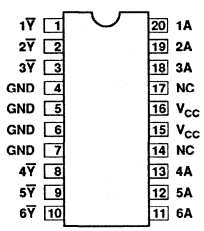
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

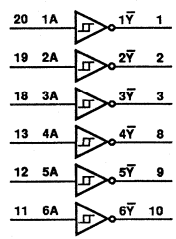
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11014N 74ACT11014N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11014D 74ACT11014D

PIN CONFIGURATION

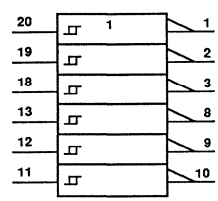
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Hex inverter Schmitt-trigger 74AC/ACT11014

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20, 19, 18, 13, 12, 11	1A - 6A	Data inputs
1, 2, 3, 8, 9, 10	$1\overline{Y}$ - $6\overline{Y}$	Data outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

INPUT	OUTPUT
nA	$n\overline{Y}$
L	H
H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11014			74ACT11014			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	0		100	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11014				74ACT11014				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{T+}	Positive-going threshold			3.0		2.2		2.2					V
				4.5		3.2		3.2		2.0		2.0	
				5.5		3.9		3.9		2.0		2.0	
V_{T-}	Negative-going threshold			3.0	0.5		0.5						V
				4.5	0.9		0.9			0.8		0.8	
				5.5	1.1		1.1			0.8		0.8	
ΔV_T	Hysteresis (V_{T+} - V_{T-})			3.0	0.3	1.2	0.3	1.2					V
				4.5	0.4	1.4	0.4	1.4	0.4	1.2	0.4	1.2	
				5.5	0.5	1.6	0.5	1.6	0.4	1.2	0.4	1.2	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		3.6		0.44					
			I_{OL} = 24mA	4.5		3.6		0.44		3.6		0.44	
				5.5		3.6		0.44		3.6		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±0.1		±0.1		±0.1	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		4.0		4.0		4.0		4.0	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	WAVEFORM	74AC11014					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.2 1.7	5.4 6.0	9.2 8.5	1.2 1.7	9.8 9.3	ns

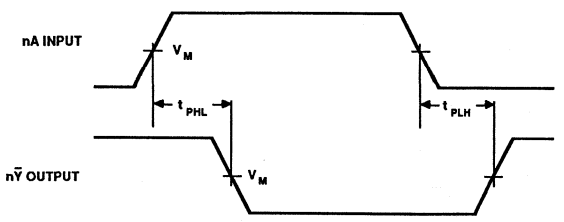
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	WAVEFORM	74AC11014					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.1 1.5	3.6 4.1	6.8 6.7	1.1 1.5	7.1 7.4	ns

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	WAVEFORM	74ACT11014					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS

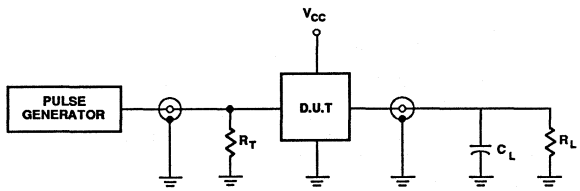


Waveform 1. Waveforms Showing the Input (nA) to Output (n$\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

Date of Issue	October 20, 1989
Status	Product Specification
ACL Products	

AC11132: Product Specification
ACT11132: Objective Specification
Quad 2-Input NAND Schmitt-trigger

FEATURES

- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: SSI

DESCRIPTION

The 74AC/ACT11132 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11132 provides four separate 2-input NAND gate functions which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay A, B, to $\overline{Y}$	C_L = 50pF	4.2	7.9	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	27	30	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

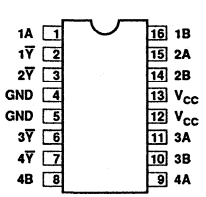
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

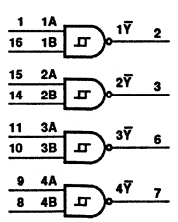
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11132N 74ACT11132N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11132D 74ACT11132D

PIN CONFIGURATION

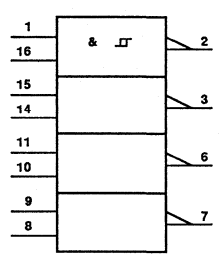
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Quad 2-Input NAND Schmitt-trigger 74AC/ACT11132

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	$n\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	AC11132			ACT11132			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	0		100	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11132				74ACT11132				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{T+}	Positive-going threshold			3.0		2.2		2.2					V
				4.5		3.2		3.2		2.0		2.0	
				5.5		3.9		3.9		2.0		2.0	
V_{T-}	Negative-going threshold			3.0	0.5		0.5						V
				4.5	0.9		0.9			0.8		0.8	
				5.5	1.1		1.1			0.8		0.8	
ΔV_T	Hysteresis (V_{T+} - V_{T-})			3.0	0.3	1.2	0.3	1.2					V
				4.5	0.4	1.4	0.4	1.4	0.4	1.2	0.4	1.2	
				5.5	0.5	1.6	0.5	1.6	0.4	1.2	0.4	1.2	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		3.6		0.44					
			I_{OL} = 24mA	4.5		3.6		0.44		3.6		0.44	
				5.5		3.6		0.44		3.6		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±0.1		±0.1		±0.1	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		4.0		4.0		4.0		4.0	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11132					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	2.2 2.8	6.2 6.8	9.2 9.8	2.2 2.8	10.3 10.5	ns

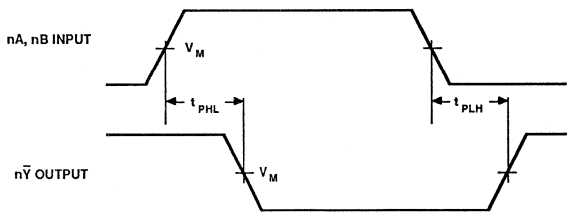
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11132					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.8 2.3	4.2 4.8	6.9 7.3	1.8 2.3	7.5 8.0	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11132					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.5			1.5 1.5		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (nA, nB) to Output (n$\overline{Y}$) Propagation Delays

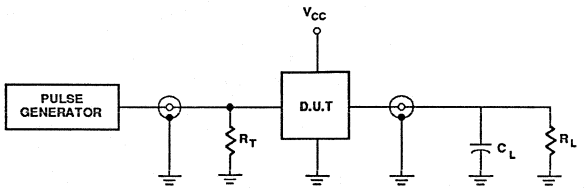
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

Quad 2-Input NAND Schmitt-trigger

74AC/ACT11132

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	May 11, 1990
Status	Product Specification
ACL Products	

AC11139: Product Specification
ACT11139: Preliminary Specification
Dual 2-to-4 line decoder/ demultiplexer; active-Low

FEATURES

- Demultiplexing capability
- Two independent 1-of-4 decoders
- Inverting outputs
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11139 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11139 has two independent decoders, each accepting two binary weighted inputs (nA_0, nA_1) and providing four mutually exclusive active-Low outputs ($n\overline{Y}_0$ - $n\overline{Y}_3$). Each decoder has an active-Low Enable ($n\overline{E}$). When $\overline{E}$ is High, every output is forced High. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay nA_n to $n\overline{Y}_n$	C_L = 50pF	3.8	5.6	ns
C_{PD}	Power dissipation capacitance per decoder[1]	f = 1MHz; C_L = 50pF	46	47	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

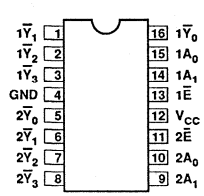
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

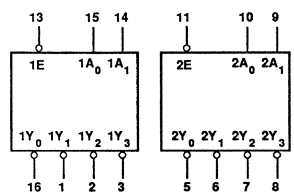
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11139N 74ACT11139N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11139D 74ACT11139D

PIN CONFIGURATION

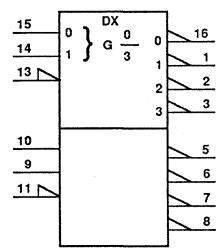
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Dual 2-to-4 line decoder/demultiplexer; active-Low 74AC/ACT11139

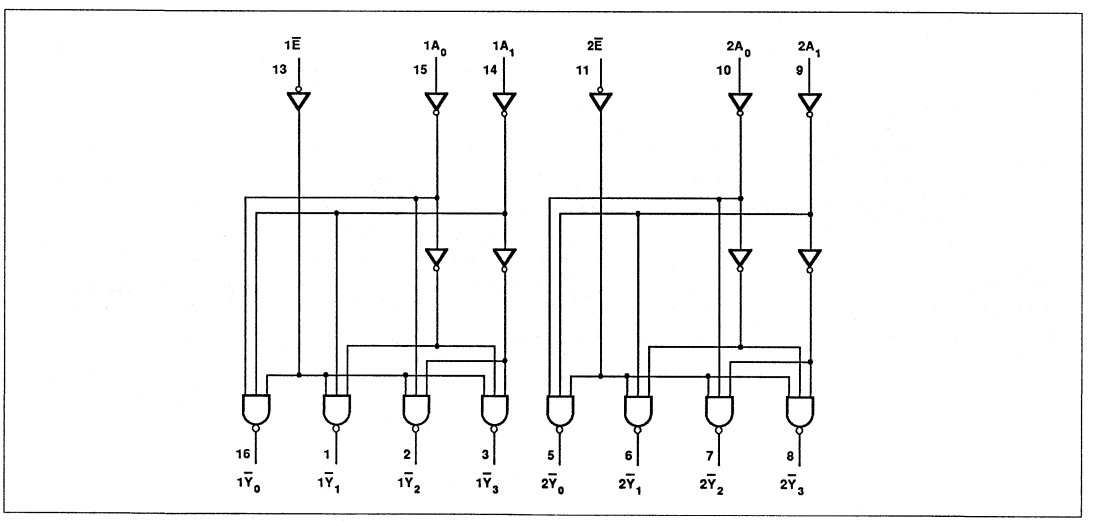
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15, 14	$1A_0$, $1A_1$	Address inputs, decoder 1
13	$1\overline{E}$	Enable input (active Low), decoder 1
16, 1, 2, 3	$1\overline{Y}_0$ to $1\overline{Y}_3$	Outputs, decoder 1
10, 9	$2A_0$, $2A_1$	Address inputs, decoder 2
11	$2\overline{E}$	Enable input (active Low), decoder 2
5, 6, 7, 8	$2\overline{Y}_0$ to $2\overline{Y}_3$	Outputs, decoder 2
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11139			74ACT11139			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Dual 2-to-4 line decoder/demultiplexer; active-Low 74AC/ACT11139

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11139				74ACT11139				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Dual 2-to-4 line decoder/demultiplexer; active-Low 74AC/ACT11139

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11139					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA_n to $n\overline{Y}_n$	1 and 2	1.5 1.5	5.3 6.0	8.1 8.4	1.5 1.5	9.0 9.4	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to $n\overline{Y}_n$	2	1.5 1.5	5.3 5.6	6.9 7.4	1.5 1.5	7.6 8.1	ns

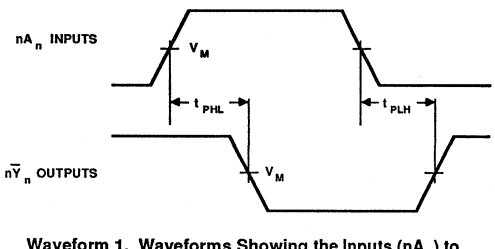
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11139					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA_n to $n\overline{Y}_n$	1 and 2	1.5 1.5	3.5 4.1	6.0 6.3	1.5 1.5	6.6 6.9	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to $n\overline{Y}_n$	2	1.5 1.5	3.8 4.0	5.2 5.6	1.5 1.5	5.7 6.2	ns

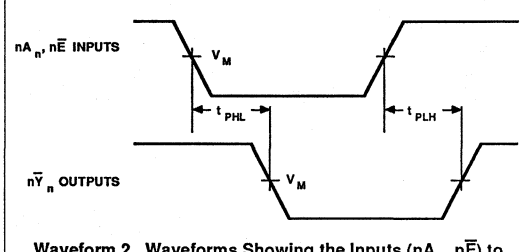
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11139					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA_n to $n\overline{Y}_n$	1 and 2	1.7 2.2	5.6 5.5	7.2 7.0	1.7 2.2	7.8 7.7	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to $n\overline{Y}_n$	2	2.8 2.1	5.2 4.9	6.7 6.3	2.8 2.1	7.3 6.9	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Inputs (nA_n) to Output ($n\overline{Y}_n$) Propagation Delays



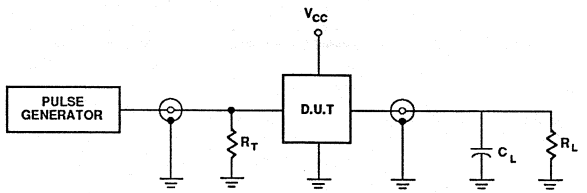
Waveform 2. Waveforms Showing the Inputs (nA_n, $n\overline{E}$) to Output ($n\overline{Y}_n$) Propagation Delays

Dual 2-to-4 line decoder/demultiplexer; active-Low 74AC/ACT11139

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11153

Dual 4-input multiplexer

FEATURES

- Separate Output Enable inputs for each section
- Common Select inputs
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11153 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11153 device provides two identical 4-input multiplexers with non-inverting outputs which select two bits from four sources selected by common select inputs (S_0, S_1). When the individual Enable ($1\overline{E}$, $2\overline{E}$) inputs of the 4-input multiplexers are High, the outputs are forced Low.

The 74AC/ACT11153 devices are the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two select inputs.

The '11153 is the non-inverting version of the '11352.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay $1I_n$, $2I_n$ to nY	C_L = 50pF	4.7	5.9	ns
C_{PD}	Power dissipation capacitance per multiplexer[1]	f = 1MHz; C_L = 50pF	30	34	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

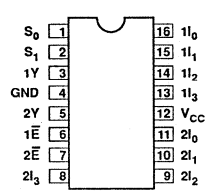
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

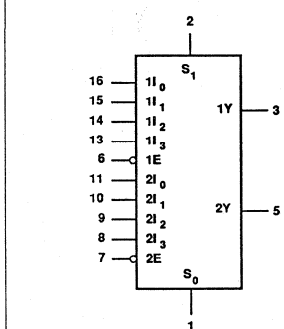
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11153N 74ACT11153N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11153D 74ACT11153D

PIN CONFIGURATION

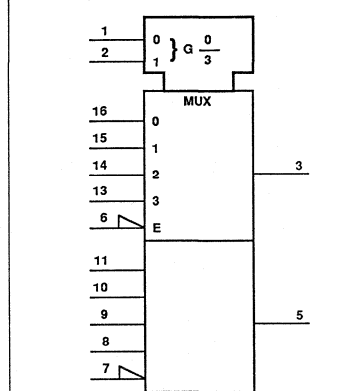
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Dual 4-input multiplexer

74AC/ACT11153

PIN DESCRIPTION

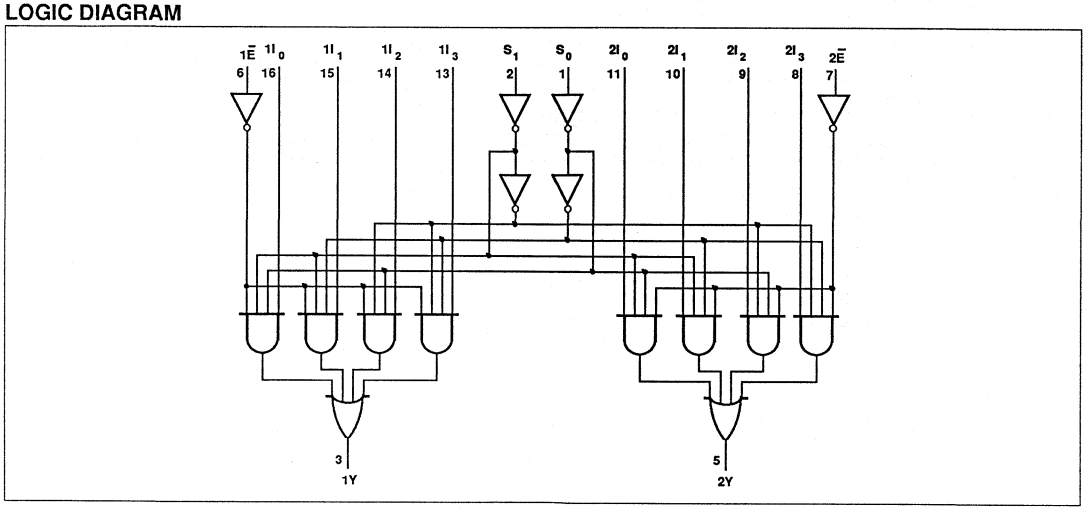
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2	S_0, S_1	Common select inputs
16, 15, 14, 13	$1I_0$ - $1I_3$	Port A data inputs
11, 10, 9, 8	$2I_0$ - $2I_3$	Port B data inputs
6	$1\overline{E}$	Port A enable input (active Low)
7	$2\overline{E}$	Port B enable input (active Low)
3, 5	1Y, 2Y	Data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS							OUTPUT
$n\overline{E}$	S_0	S_1	nI_0	nI_1	nI_2	nI_3	nY
H	X	X	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
L	H	L	X	L	X	X	L
L	H	L	X	H	X	X	H
L	L	H	X	X	L	X	L
L	L	H	X	X	H	X	H
L	H	H	X	X	X	L	L
L	H	H	X	X	X	H	H

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
Z = High-impedance "OFF" state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	AC11153			ACT11153			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11153				74ACT11153				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11153					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_n to nY	1	2.3 2.6	6.9 7.1	8.4 8.7	2.3 2.6	9.5 9.9	ns
t_{PLH} t_{PHL}	Propagation delay S_n to nY	1	2.3 2.6	7.4 7.6	9.5 9.9	2.3 2.6	10.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to nY	2	1.8 1.0	5.3 5.2	6.7 7.2	1.8 1.0	7.5 8.5	ns

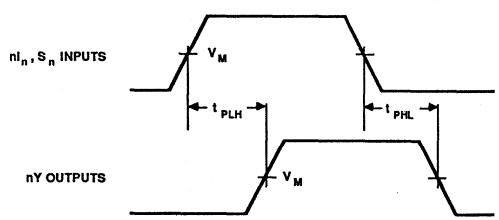
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11153					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_n to nY	1	1.9 2.5	4.5 5.0	6.1 6.9	1.9 2.5	6.9 7.8	ns
t_{PLH} t_{PHL}	Propagation delay S_n to nY	1	2.0 1.6	4.7 5.5	6.8 7.7	2.0 1.6	7.6 8.6	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to nY	2	1.4 1.8	3.6 4.3	5.1 5.8	1.4 1.8	5.7 6.7	ns

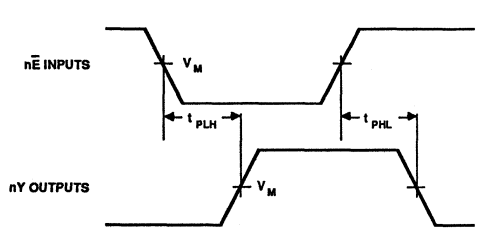
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11153					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_n to nY	1	2.8 3.0	5.4 6.4	7.5 8.8	2.8 3.0	8.3 9.8	ns
t_{PLH} t_{PHL}	Propagation delay S_n to nY	1	2.8 3.1	6.4 6.8	9.8 10.0	2.8 3.1	10.9 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to nY	2	2.2 2.9	5.5 5.6	8.6 6.6	2.2 2.9	9.3 7.6	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Data Inputs (nI_n) and Select Input (S_n) to Output (nY) Propagation Delays

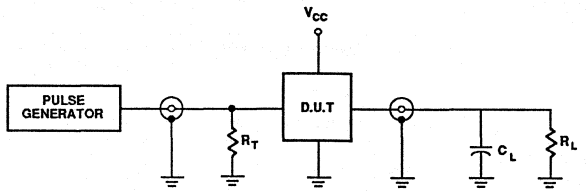


Waveform 2. Waveforms Showing the Enable Input ($n\overline{E}$) to Output (nY) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11157
Quad 2-input multiplexer

FEATURES

- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11157 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11157 provides four 2-to-1 multiplexers with a common selector and a common enable. The state of the Select (S) input determines the particular input from which the data comes. The Enable (E) input is active-Low. When E is High, all of the outputs (Y) are forced Low regardless of all other input conditions.

The device is the logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the Select input.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay nI_0, nI_1 to nY	C_L = 50pF	4.6	5.9	ns
C_{PD}	Power dissipation capacitance per mulitplexer[1]	f = 1MHz; C_L = 50pF	36	36	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

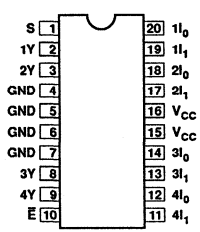
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_o = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

ORDERING INFORMATION

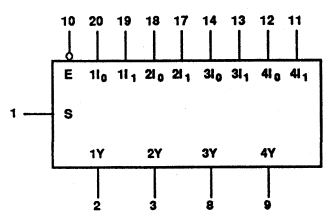
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11157N 74ACT11157N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11157D 74ACT11157D

PIN CONFIGURATION

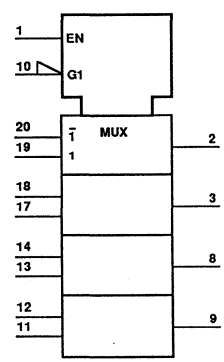
N and D Packages



LOGIC SYMBOL



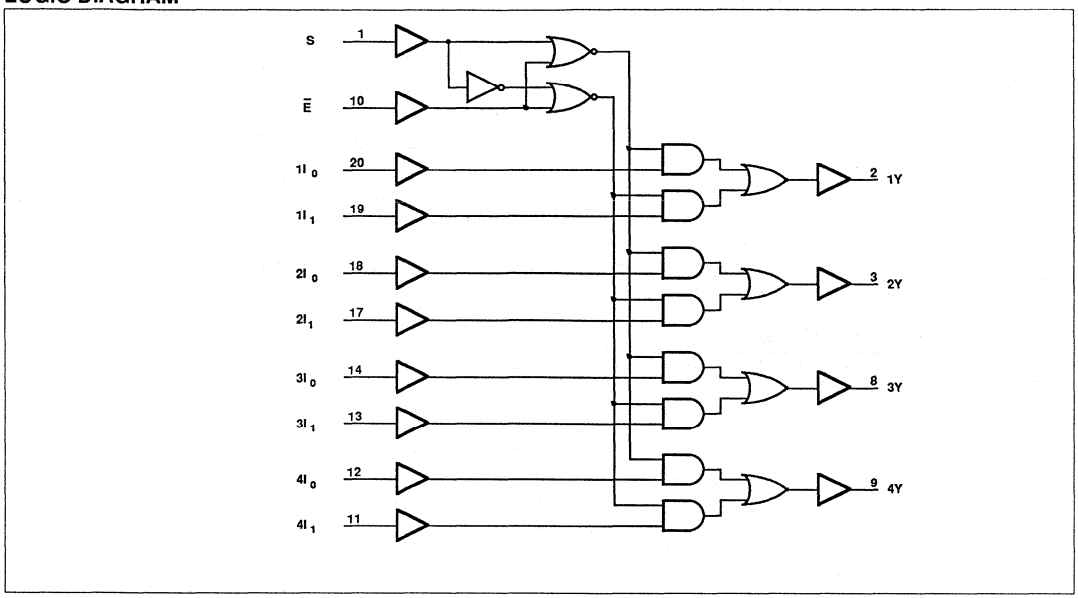
LOGIC SYMBOL (IEEE/IEC)



Quad 2-input multiplexer

74AC/ACT11157

LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	S	Common select input
20, 18, 14, 12	$1I_0$ - $4I_0$	Data inputs
19, 17, 13, 11	$1I_1$ - $4I_1$	Data inputs
2, 3, 8, 9	1Y - 4Y	Data outputs
10	$\overline{E}$	Output enable input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	nI_0	nI_1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11157			74ACT11157			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11157				74ACT11157				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11157					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to nY	1	1.8 2.6	6.2 8.3	8.5 11.1	1.8 2.9	9.5 12.5	ns
t_{PLH} t_{PHL}	Propagation delay S to nY	1	1.9 2.7	6.8 8.7	8.9 11.4	1.9 2.7	10.0 12.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to nY	2	1.6 2.8	6.0 8.6	8.6 11.2	1.6 2.8	9.2 12.3	ns

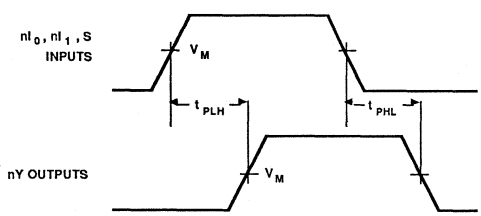
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11157					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to nY	1	1.5 2.2	3.9 5.3	5.8 7.5	1.5 2.2	6.4 8.6	ns
t_{PLH} t_{PHL}	Propagation delay S to nY	1	1.7 2.3	4.2 5.5	6.2 8.0	1.7 2.3	6.8 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to nY	2	1.6 2.3	3.8 5.4	5.9 7.8	1.6 2.3	6.5 8.8	ns

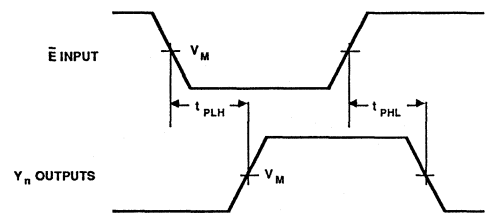
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11157					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to nY	1	2.6 3.1	5.1 6.6	7.1 10.4	2.6 3.1	7.8 11.3	ns
t_{PLH} t_{PHL}	Propagation delay S to nY	1	2.3 3.1	5.6 6.8	8.7 10.5	2.3 3.1	9.5 11.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to nY	2	2.1 3.6	5.1 6.9	7.9 9.7	2.1 3.6	8.6 10.8	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Data Inputs (nI_0, nI_1) and Select Input (S) to Output ($n\overline{Y}$) Propagation Delays



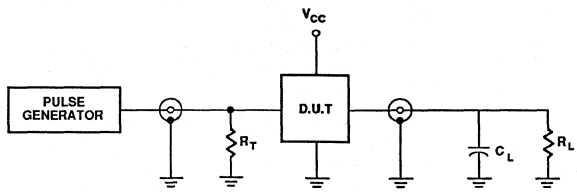
Waveform 2. Waveforms Showing the Enable Input ($\overline{E}$) to Output ($n\overline{Y}$) Propagation Delays

Quad 2-input multiplexer 74AC/ACT11157

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11158

Quad 2-input multiplexer, INV

FEATURES

- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11158 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11158 provides four 2-to-1 multiplexers with a common selector and a common enable. The state of the Select (S) input determines the particular register from which the data comes. The Enable ($\overline{E}$) input is active-Low. When $\overline{E}$ is High, all of the inverting outputs ($\overline{Y}$) are forced High regardless of all other input conditions.

The device is the logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the Select input.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	C_L = 50pF	3.8	5.5	ns
C_{PD}	Power dissipation capacitance per mulitplexer[1]	f = 1MHz; C_L = 50pF	33	37	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

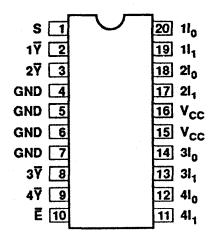
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

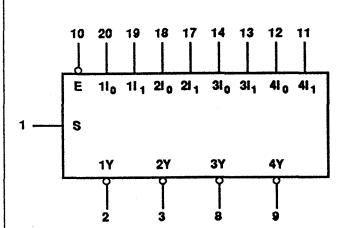
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11158N 74ACT11158N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11158D 74ACT11158D

PIN CONFIGURATION

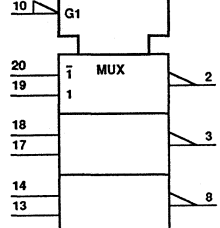
N and D Packages



LOGIC SYMBOL



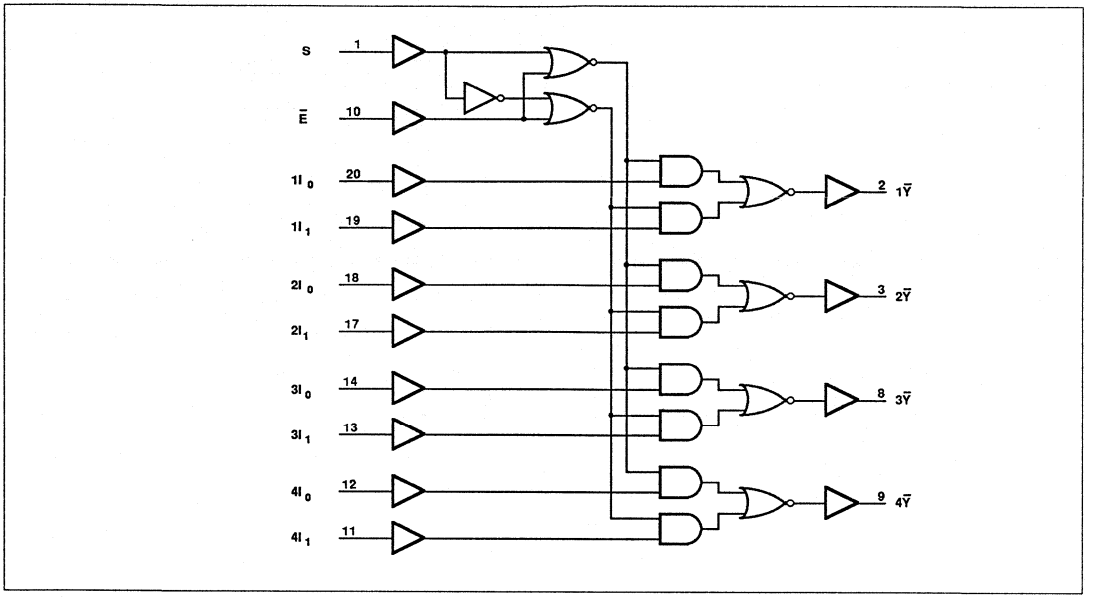
LOGIC SYMBOL (IEEE/IEC)



Quad 2-input multiplexer, INV

74AC/ACT11158

LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	S	Common select input
20, 18, 14, 12	nI_0 - nI_0	Data inputs
19, 17, 13, 11	nI_1 - nI_1	Data inputs
2, 3, 8, 9	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
10	$\overline{E}$	Output enable input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	nI_0	nI_1	$n\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11158			74ACT11158			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	0		10	ns/V
		Select and Enable	0		5	0		5	
T_{amb}	Operating free-air temperature range		-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11158				74ACT11158				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11158					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	1	1.5 1.5	5.8 5.9	7.3 7.6	1.5 1.5	8.0 8.4	ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	1	1.5 1.5	6.5 6.8	8.0 8.4	1.5 1.5	8.8 9.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $n\overline{Y}$	2	1.5 1.5	5.7 6.3	7.1 7.8	1.5 1.5	8.0 8.7	ns

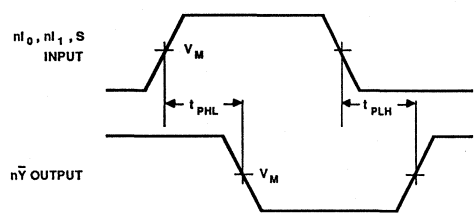
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11158					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	1	1.5 1.5	3.6 3.9	5.4 5.6	1.5 1.5	5.8 6.4	ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	1	1.5 1.5	4.1 4.4	5.9 6.2	1.5 1.5	6.4 6.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $n\overline{Y}$	2	1.5 1.5	3.7 4.2	5.4 5.9	1.5 1.5	5.9 6.5	ns

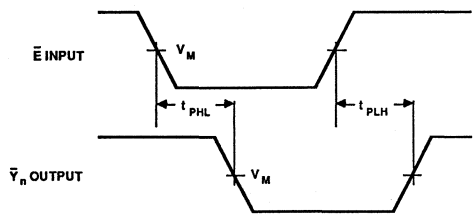
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11158					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nI_0, nI_1 to $n\overline{Y}$	1	2.0 2.7	5.1 5.9	7.6 8.3	2.0 2.7	8.4 9.4	ns
t_{PLH} t_{PHL}	Propagation delay S to $n\overline{Y}$	1	2.3 2.9	5.3 6.7	7.7 9.8	2.3 2.9	8.5 10.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to $n\overline{Y}$	2	2.5 2.5	5.1 6.1	6.8 8.9	2.5 2.5	7.5 10.0	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Data Inputs (nI_0, nI_1) and Select Input (S) to Output ($n\overline{Y}$) Propagation Delays



Waveform 2. Waveforms Showing the Enable Input ($\overline{E}$) to Output ($n\overline{Y}$) Propagation Delays

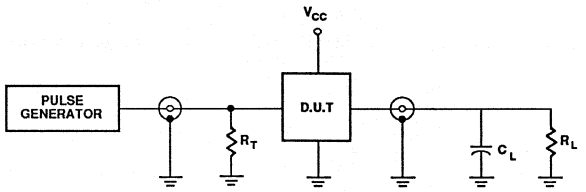
Quad 2-input multiplexer, INV

74AC/ACT11158

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11160

Synchronous presettable synchronous BCD decade counter, asynchronous reset

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous reset
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11160 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11160 4-bit synchronous presettable decade counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP_n to Q_n ($\overline{PE}$ = High)	C_L = 50pF	6.9	6.4	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	48	60	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	140	125	MHz

Note:

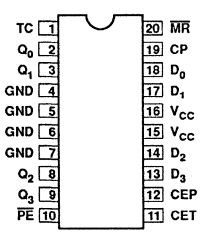
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

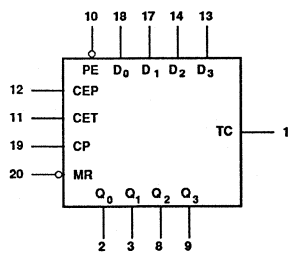
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11160N 74ACT11160N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11160D 74ACT11160D

PIN CONFIGURATION

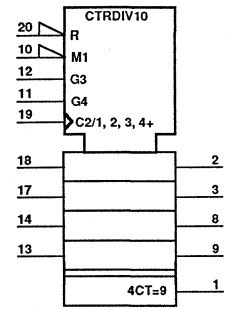
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

The outputs of the counters may be preset to High or Low levels. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the rising edge of the clock. Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels, regardless of the levels at CP, $\overline{PE}$, CET, and CEP inputs (thus providing an asynchronous clear function).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the Terminal Count (TC) output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{MR}$	Asynchronous master reset (active Low)
19	CP	Clock input (Low-to-High, edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
12	CEP	Count enable input
10	$\overline{PE}$	Parallel enable input (active Low)
11	CET	Count enable carry input
18, 17, 14, 13	Q_0 - Q_3	Counter outputs
1	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(1)
Count	H	↑	h	h	h	X	count	(1)
Hold (do nothing)	H	X	l	X	h	X	q_n	(1)
	H	X	X	l	h	X	q_n	L

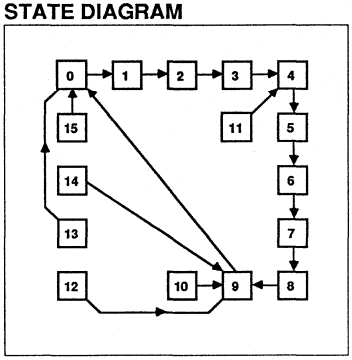
H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to High clock transition
↑ = Low-to-High clock transition

NOTE:
1. The TC output is High when CET is High and the counter is at Terminal Count (HLLH).

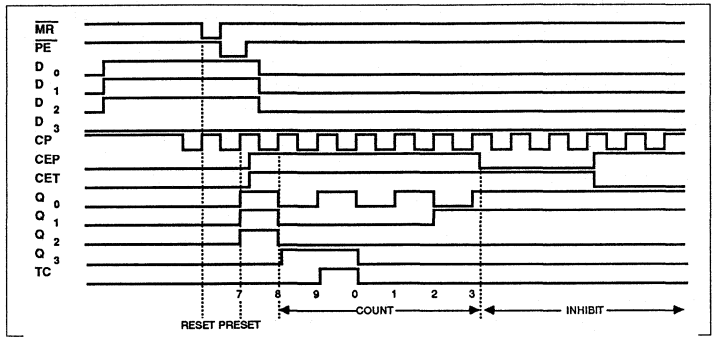
Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

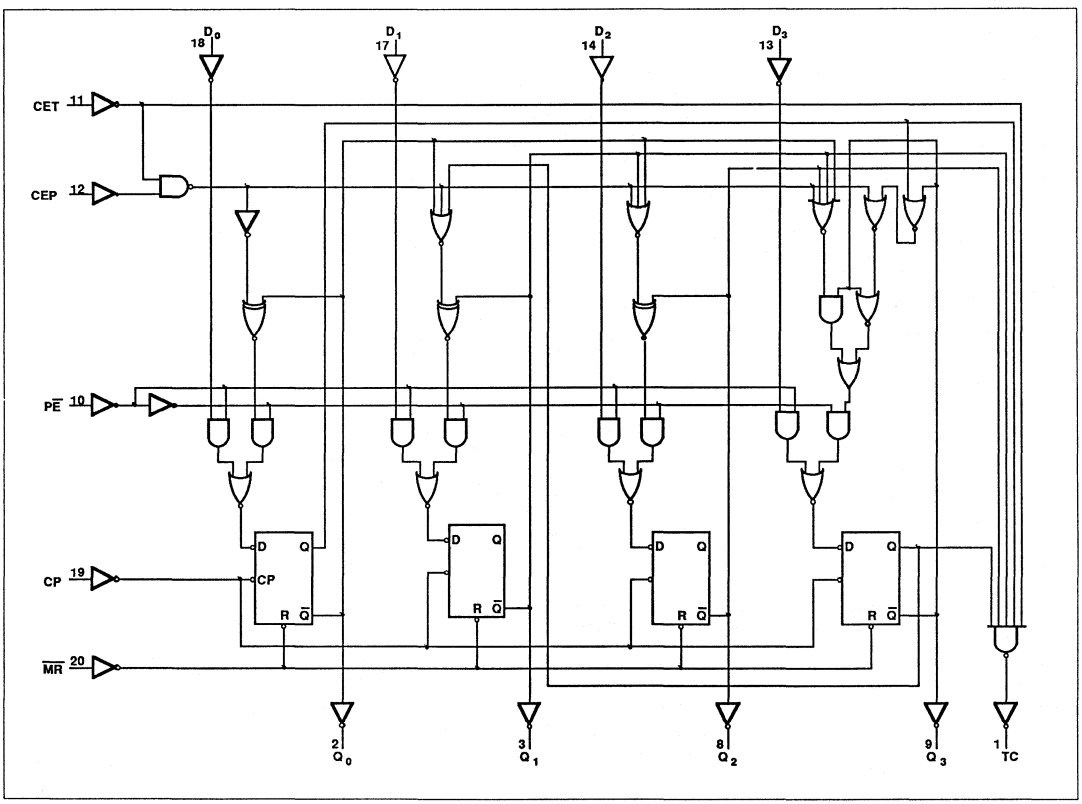
STATE DIAGRAM



TIMING DIAGRAM



LOGIC DIAGRAM



Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	AC11160			ACT11160			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11160				74ACT11160				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	WAVEFORM	74AC11160					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	66	90		66		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	9.0 10.6	11.2 13.4	1.5 1.5	12.5 15.1	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	8.6 10.1	10.8 12.8	1.5 1.5	12.1 14.4	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	11.2 12.2	13.6 15.1	1.5 1.5	15.2 17.2	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	1.5 1.5	6.0 6.8	7.6 8.9	1.5 1.5	8.3 9.9	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	12.0	15.2	1.5	17.3	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	1.5	14.1	17.3	1.5	19.7	ns
t_S	Setup time, High or Low D_n to CP	4	6.5			6.5		ns
t_H	Hold time, High or Low D_n to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4	6.5			6.5		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low CEP or CET to CP	5	6.0			6.0		ns
t_H	Hold time, High or Low CEP or CET to CP	5	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	7.5			7.5		ns
t_W	Clock pulse width (count) High or Low	1	7.5			7.5		ns
t_W	$\overline{MR}$ pulse width, Low	2	6.0			6.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	6.0			6.0		ns

Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11160					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	140		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	6.3 7.4	8.0 9.8	1.5 1.5	8.9 11.2	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	6.0 7.1	7.5 9.4	1.5 1.5	8.4 10.7	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	7.8 8.5	9.5 10.6	1.5 1.5	10.7 12.1	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	1.5 1.5	4.2 5.0	5.5 6.7	1.5 1.5	6.0 7.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	8.2	10.7	1.5	12.1	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	1.5	9.9	12.2	1.5	13.8	ns
t_S	Setup time, High or Low D_n to CP	4	3.5			3.5		ns
t_H	Hold time, High or Low D_n to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4	6.5			6.5		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low CEP or CET to CP	5	4.5			4.5		ns
t_H	Hold time, High or Low CEP or CET to CP	5	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	4.5			4.5		ns
t_W	Clock pulse width (count) High or Low	1	4.5			4.5		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	6.0			6.0		ns

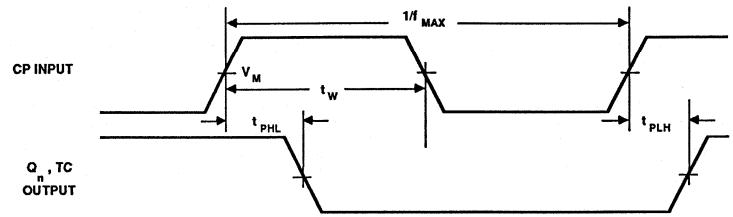
Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

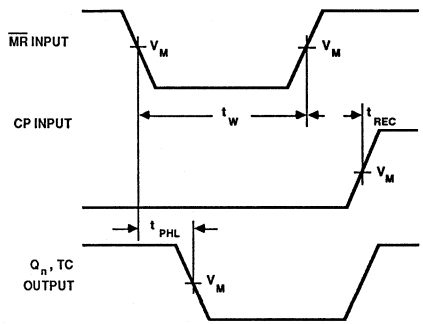
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11160					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	2.8 3.5	5.9 6.8	8.3 9.1	2.8 3.5	9.1 10.2	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	3.0 3.7	5.8 6.7	7.9 8.8	3.0 3.7	8.6 9.8	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	3.8 4.4	6.9 8.3	9.1 10.8	3.8 4.4	10.1 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	2.3 3.1	4.3 6.7	5.6 9.2	2.3 3.1	6.0 10.1	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	4.4	8.7	11.9	4.4	13.2	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	5.4	10.1	13.2	5.4	14.7	ns
t_S	Setup time, High or Low D_n to CP	4	5.5			5.5		ns
t_H	Hold time, High or Low D_n to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4	7.0			7.0		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low CEP or CET to CP	5	7.0			7.0		ns
t_H	Hold time, High or Low CEP or CET to CP	5	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	5.0			5.0		ns
t_W	Clock pulse width (count) High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	5.0			5.0		ns

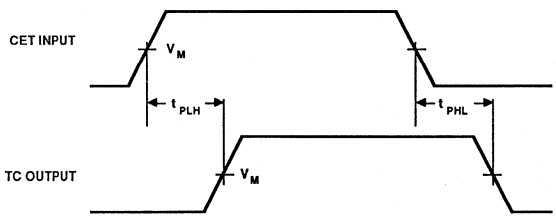
AC WAVEFORMS



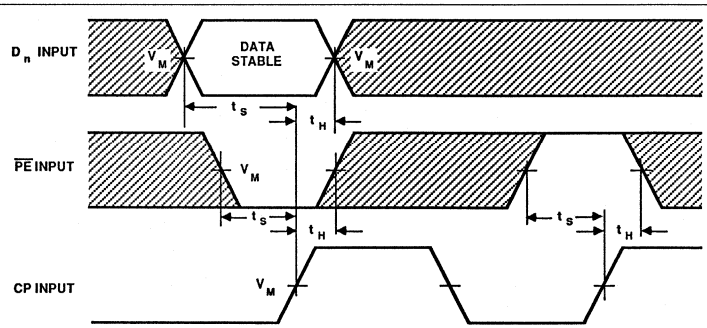
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Master Reset ($\overline{MR}$) Pulse Width, the Master Reset to Output (Qn, TC) Propagation Delays, and the Master Reset to Clock (CP) Recovery Time

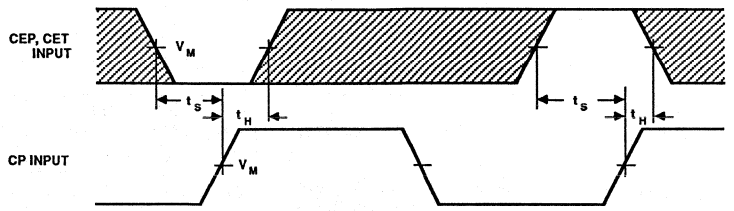


Waveform 3. Waveforms Showing the Input (CET) to Output (TC) Propagation Delays



Waveform 4. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n) and Parallel Enable Input $\overline{PE}$

AC WAVEFORMS (Continued)

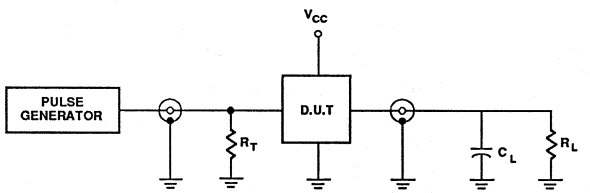


Waveform 5. Waveforms Showing CEP and CET Set-up and Hold Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	May 21, 1990
Status	Preliminary Specification
ACL Products	

74AC/ACT11161

Synchronous presettable synchronous 4-bit binary counter, asynchronous reset

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous reset
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11161 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11161 4-bit synchronous presettable binary counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP_n to Q_n ($\overline{PE}$ = High)	C_L = 50pF	5.5	6.2	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	51	51	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	185	140	MHz

Note:

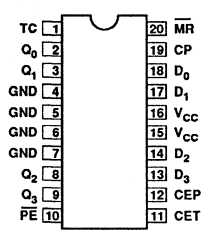
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

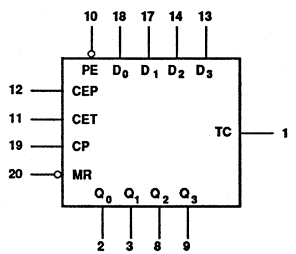
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11161N 74ACT11161N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11161D 74ACT11161D

PIN CONFIGURATION

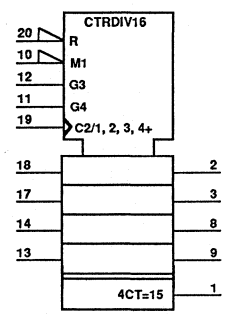
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Synchronous presettable synchronous 4-bit binary counter, asynchronous reset

74AC/ACT11161

The outputs of the counters may be preset to High or Low levels. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the rising edge of the clock. Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels, regardless of the levels at CP, $\overline{PE}$, CET, and CEP inputs (thus providing an asynchronous clear function).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the Terminal Count (TC) output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{MR}$	Asynchronous master reset (active Low)
19	CP	Clock input (Low-to-High, edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
12	CEP	Count enable input
10	$\overline{PE}$	Parallel enable input (active Low)
11	CET	Count enable carry input
2, 3, 8, 9	Q_0 - Q_3	Counter outputs
1	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(1)
Count	H	↑	h	h	h	X	count	(1)
Hold (do nothing)	H	X	l	X	h	X	q_n	(1)
	H	X	X	l	h	X	q_n	L

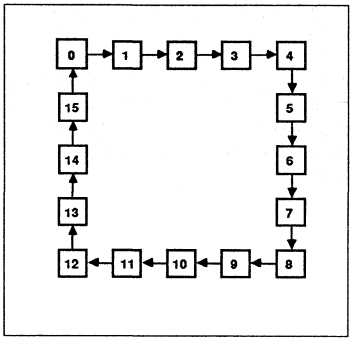
H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to High clock transition
↑ = Low-to-High clock transition

NOTE:
1. The TC output is High when CET is High and the counter is at Terminal Count (HHHH).

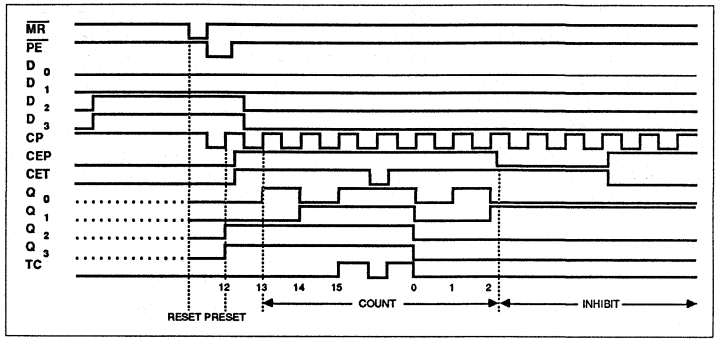
Synchronous presettable synchronous 4-bit binary counter, asynchronous reset

74AC/ACT11161

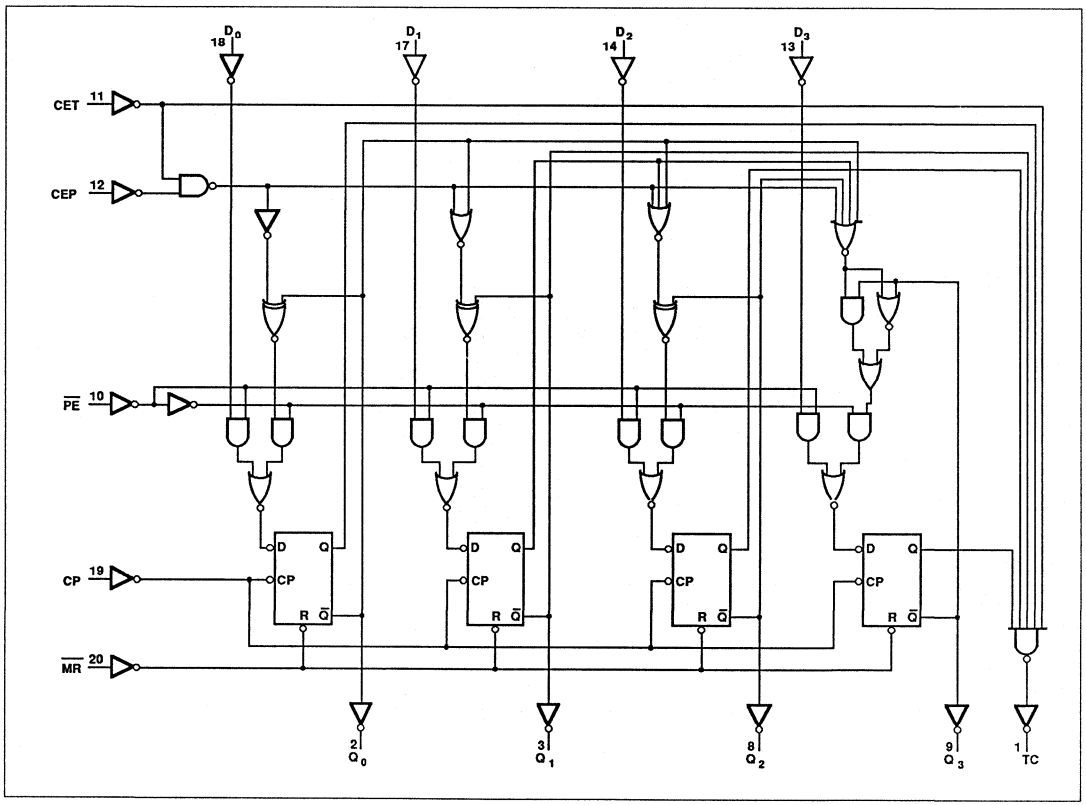
STATE DIAGRAM



TIMING DIAGRAM



LOGIC DIAGRAM



Synchronous presettable synchronous 4-bit binary counter, asynchronous reset

74AC/ACT11161

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11161			74ACT11161			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Synchronous presettable synchronous 4-bit binary counter, asynchronous reset

74AC/ACT11161

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11161				74ACT11161				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Synchronous presettable synchronous 4-bit binary counter, asynchronous reset

74AC/ACT11161

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11161					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	3.0 3.6	7.9 8.8	9.8 10.8	3.0 3.6	10.9 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	2.9 3.4	7.8 8.6	9.6 10.6	2.9 3.4	10.7 11.8	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	4.0 4.9	10.0 11.3	12.1 13.8	4.0 4.9	13.3 15.4	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	2.0 2.5	5.7 6.2	7.2 7.7	2.0 2.5	7.9 8.4	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	3.8	9.3	11.3	3.8	12.7	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	5.2	12.0	14.3	5.2	15.8	ns
t_S	Setup time, High or Low D_n to CP	4	4.5			4.5		ns
t_H	Hold time, High or Low D_n to CP	4	1.5			1.5		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4	6.5			6.5		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4	2.0			2.0		ns
t_S	Setup time, High or Low CEP or CET to CP	5	6.5			6.5		ns
t_H	Hold time, High or Low CEP or CET to CP	5	1.5			1.5		ns
t_W	Clock pulse width (load) High or Low	1	4.0			4.0		ns
t_W	Clock pulse width (count) High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.8			4.8		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	6.5			6.5		ns

Synchronous presettable synchronous 4-bit binary counter, asynchronous reset

74AC/ACT11161

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11161					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	185		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	2.5 3.0	5.0 5.9	6.9 8.0	2.5 3.0	7.6 8.9	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	2.5 3.0	4.9 5.7	6.8 7.6	2.5 3.0	7.5 8.6	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	3.4 4.3	6.3 7.5	8.5 10.1	3.4 4.3	9.3 11.3	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	1.7 2.3	3.7 4.3	5.3 5.9	1.7 2.3	5.6 6.4	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	3.5	6.3	8.2	3.5	9.2	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	4.9	7.9	10.1	4.9	11.3	ns
t_S	Setup time, High or Low D_n to CP	4	3.0			3.0		ns
t_H	Hold time, High or Low D_n to CP	4	1.5			1.5		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4	4.5			4.5		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4	1.5			1.5		ns
t_S	Setup time, High or Low CEP or CET to CP	5	4.5			4.5		ns
t_H	Hold time, High or Low CEP or CET to CP	5	1.5			1.5		ns
t_W	Clock pulse width (load) High or Low	1	4.0			4.0		ns
t_W	Clock pulse width (count) High or Low	1	4.0			4.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	3.7			3.7		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	4.6			4.6		ns

Synchronous presettable synchronous 4-bit binary counter, asynchronous reset

74AC/ACT11161

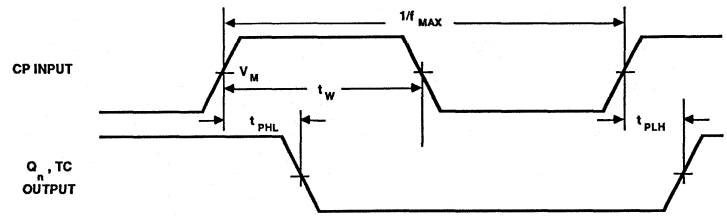
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11161					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	105	140		105		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	3.0 3.6	5.7 6.6	7.9 8.7	3.0 3.6	8.8 9.7	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	3.0 3.5	5.6 6.5	7.6 8.5	3.0 3.5	8.4 9.6	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	3.6 5.0	6.6 8.2	8.7 10.4	3.6 5.0	9.6 11.7	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	2.0 3.1	4.0 6.4	5.6 9.0	2.0 3.1	6.2 9.9	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	4.6	8.5	11.6	4.6	12.9	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	5.8	10.0	13.0	5.8	14.5	ns
t_S	Setup time, High or Low D_n to CP	4	5.0			5.0		ns
t_H	Hold time, High or Low D_n to CP	4	0.5			0.5		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4	6.5			6.5		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4	0.5			0.5		ns
t_S	Setup time, High or Low CEP or CET to CP	5	7.0			7.0		ns
t_H	Hold time, High or Low CEP or CET to CP	5	0.5			0.5		ns
t_W	Clock pulse width (load) High or Low	1	4.8			4.8		ns
t_W	Clock pulse width (count) High or Low	1	4.7			4.7		ns
t_W	$\overline{MR}$ pulse width, Low	2	6.5			6.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	4.5			4.5		ns

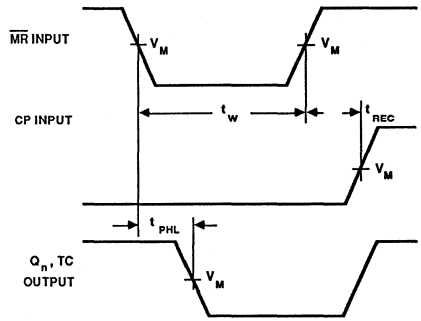
Synchronous presettable synchronous 4-bit binary counter, asynchronous reset

74AC/ACT11161

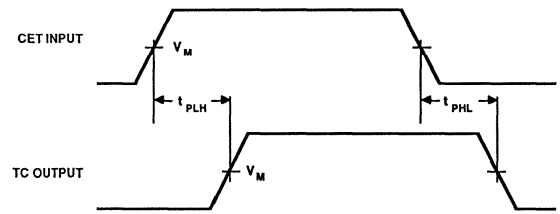
AC WAVEFORMS



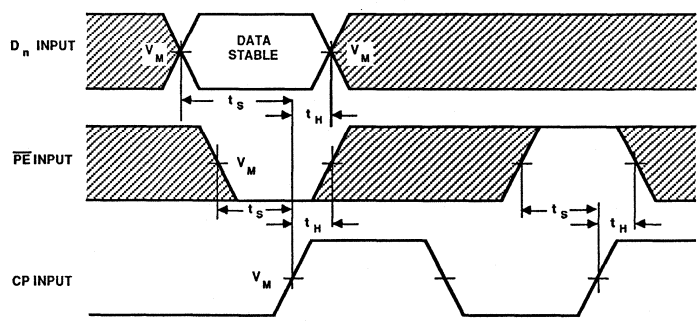
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Master Reset ($\overline{MR}$) Pulse Width, the Master Reset to Output (Qn, TC) Propagation Delays, and the Master Reset to Clock (CP) Recovery Time

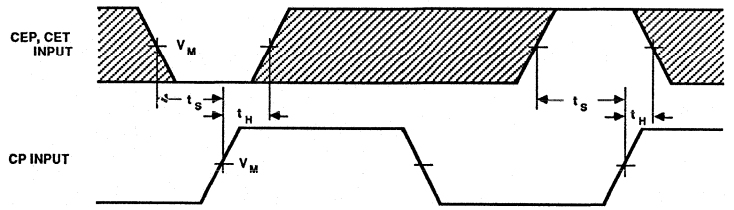


Waveform 3. Waveforms Showing the Input (CET) to Output (TC) Propagation Delays



Waveform 4. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n) and Parallel Enable Input $\overline{PE}$

AC WAVEFORMS (Continued)

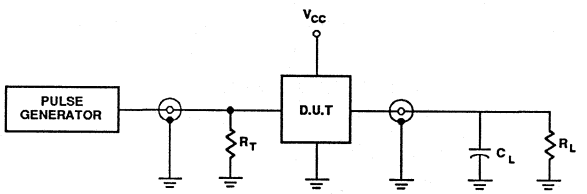


Waveform 5. Waveforms Showing CEP and CET Set-up and Hold Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11162

Synchronous presettable BCD decade counter, synchronous reset

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Synchronous reset
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11162 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11162 4-bit synchronous presettable decade counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP_n to Q_n ($\overline{PE}$ = High)	C_L = 50pF	6.9	6.2	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	54	58	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	140	150	MHz

Note:

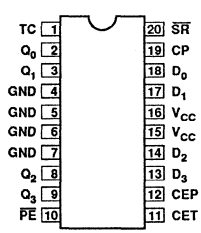
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

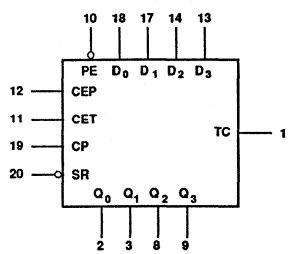
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11162N 74ACT11162N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11162D 74ACT11162D

PIN CONFIGURATION

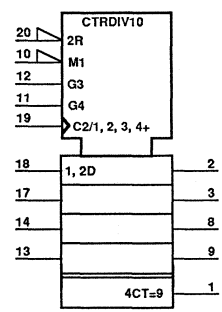
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Synchronous presettable BCD decade counter, synchronous reset

74AC/ACT11162

The outputs of the counters may be preset to High or Low levels. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the rising edge of the clock. Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels after the next positive-going transition on the clock (CP) input. This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the Terminal Count (TC) output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{SR}$	Synchronous reset (active Low)
19	CP	Clock input (Low-to-High edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
12	CEP	Count enable input
10	$\overline{PE}$	Parallel enable input (active Low)
11	CET	Count enable carry input
18, 17, 14, 13	Q_0 - Q_3	Counter outputs
1	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	(1)
Count	h	↑	h	h	h	X	count	(1)
Hold (do nothing)	h	X	l	X	h	X	q_n	(1)
	h	X	X	l	h	X	q_n	L

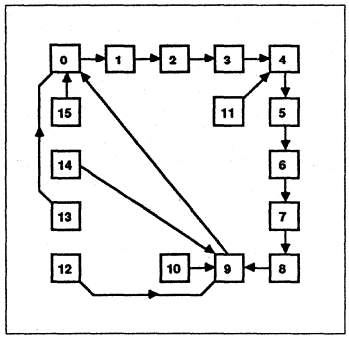
H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to High clock transition
↑ = Low-to-High clock transition

NOTE:
1. The TC output is High when CET is High and the counter is at Terminal Count (HLLH).

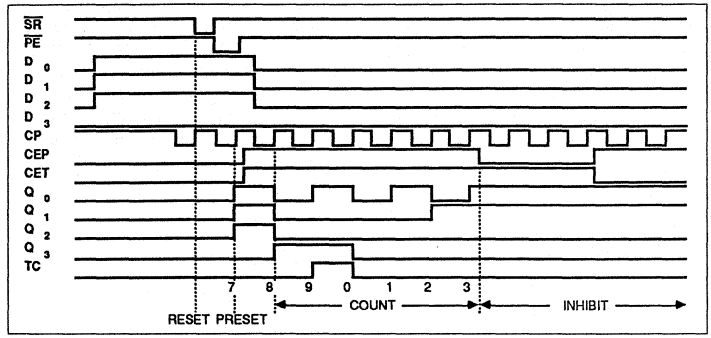
Synchronous presettable BCD decade counter, synchronous reset

74AC/ACT11162

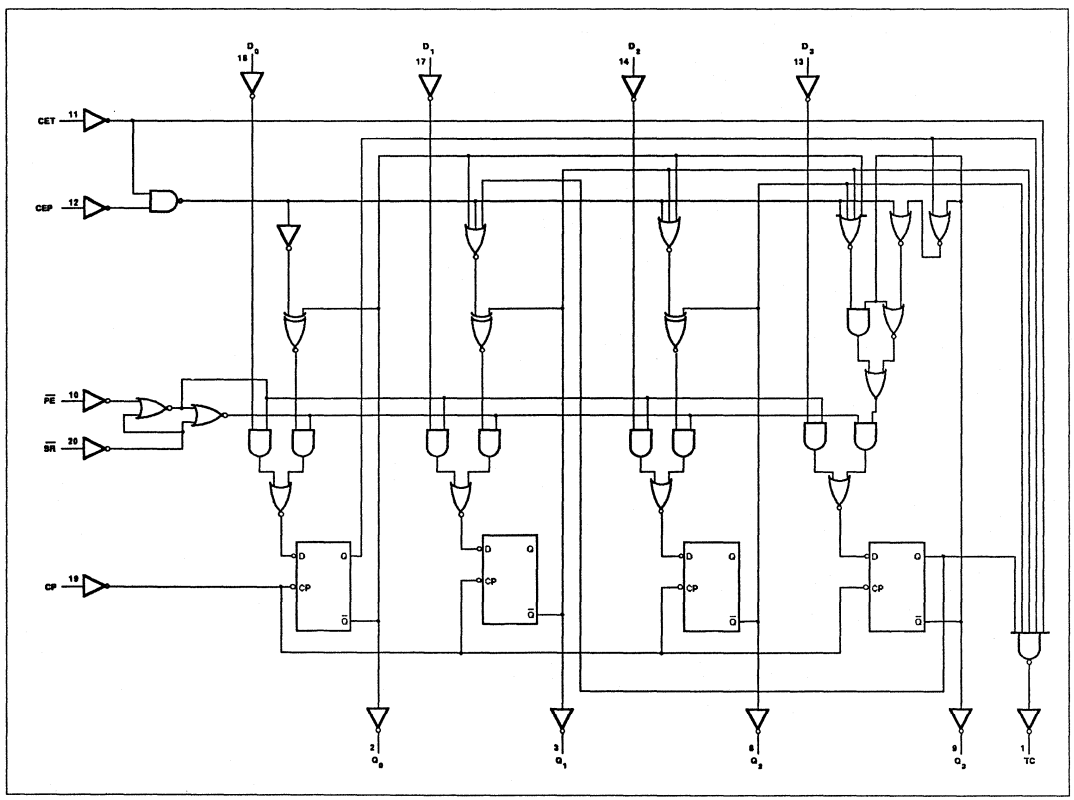
STATE DIAGRAM



TIMING DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11162			74ACT11162			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Synchronous presettable BCD decade counter, synchronous reset

74AC/ACT11162

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11162				74ACT11162				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Synchronous presettable BCD decade counter, synchronous reset

74AC/ACT11162

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11162					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	66	90		66		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	8.7 10.2	11.7 14.4	1.5 1.5	13.2 16.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	8.7 10.4	11.2 14.1	1.5 1.5	12.6 16.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	10.5 12.1	14.1 15.8	1.5 1.5	15.9 18.0	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	2	1.5 1.5	5.8 6.9	7.6 9.9	1.5 1.5	8.5 11.0	ns
t_S	Setup time, High or Low D_n to CP	3	6.0			6.0		ns
t_H	Hold time, High or Low D_n to CP	3	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	3	6.0			6.0		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	3	1.0			1.0		ns
t_S	Setup time, High or Low CEP or CET to CP	4	7.5			7.5		ns
t_H	Hold time, High or Low CEP or CET to CP	4	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	7.5			7.5		ns
t_W	Clock pulse width (count) High or Low	1	7.5			7.5		ns
t_S	Setup time, High or Low $\overline{SR}$ to CP	3	7.5			7.5		ns
t_H	Hold time, High or Low $\overline{SR}$ to CP	3	1.0			1.0		ns

Synchronous presettable BCD decade counter, synchronous reset

74AC/ACT11162

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11162					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	140		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	6.4 7.4	8.4 10.5	1.5 1.5	9.5 11.9	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	6.0 7.2	7.9 10.1	1.5 1.5	9.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	7.7 8.3	10.1 11.1	1.5 1.5	11.2 12.6	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	2	1.5 1.5	4.0 5.0	5.5 7.4	1.5 1.5	6.0 10.2	ns
t_S	Setup time, High or Low D_n to CP	3	4.0			4.0		ns
t_H	Hold time, High or Low D_n to CP	3	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	3	5.0			5.0		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	3	1.0			1.0		ns
t_S	Setup time, High or Low CEP or CET to CP	4	6.0			6.0		ns
t_H	Hold time, High or Low CEP or CET to CP	4	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	4.5			4.5		ns
t_W	Clock pulse width (count) High or Low	1	4.5			4.5		ns
t_S	Setup time, High or Low $\overline{SR}$ to CP	3	4.5			4.5		ns
t_H	Hold time, High or Low $\overline{SR}$ to CP	3	1.0			1.0		ns

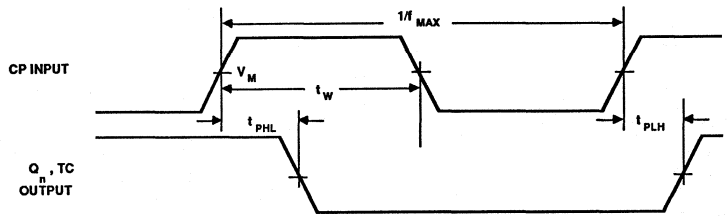
Synchronous presettable BCD decade counter, synchronous reset

74AC/ACT11162

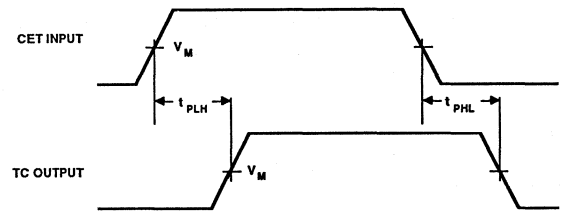
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11162					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	150		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	2.4 2.8	5.7 6.6	9.0 10.2	2.4 2.8	10.0 11.6	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	2.3 2.9	5.6 6.6	8.6 10.0	2.3 2.9	9.7 11.4	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	2.6 3.2	6.7 7.9	10.1 11.9	2.6 3.2	11.4 13.5	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	2	1.2 2.1	4.0 6.3	6.0 10.0	1.2 2.1	6.6 11.3	ns
t_S	Setup time, High or Low D_n to CP	3	5.0			5.0		ns
t_H	Hold time, High or Low D_n to CP	3	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	3	7.0			7.0		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	3	0.5			0.5		ns
t_S	Setup time, High or Low CEP or CET to CP	4	7.5			7.5		ns
t_H	Hold time, High or Low CEP or CET to CP	4	0.5			0.5		ns
t_W	Clock pulse width (load) High or Low	1	4.0			4.0		ns
t_W	Clock pulse width (count) High or Low	1	4.0			4.0		ns
t_S	Setup time, High or Low $\overline{SR}$ to CP	3	7.5			7.5		ns
t_H	Hold time, High or Low $\overline{SR}$ to CP	3	0.5			0.5		ns

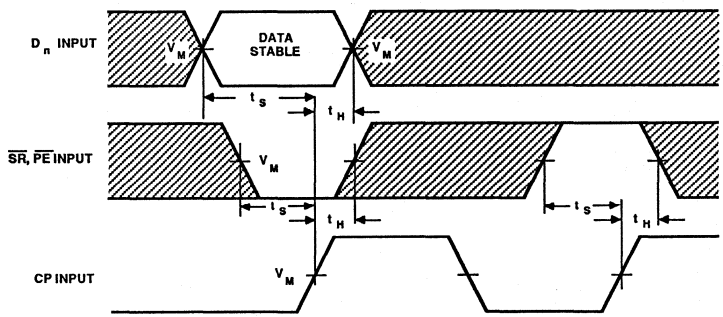
AC WAVEFORMS



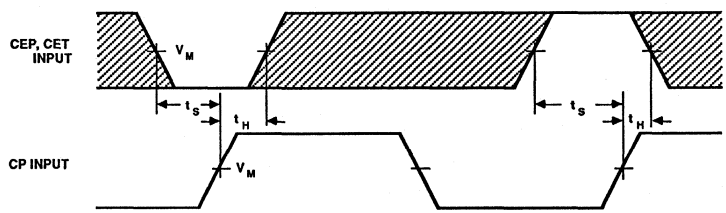
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays, and Clock Pulse Width



Waveform 2. Waveforms Showing the Input (CET) to Output (TC) Propagation Delays



Waveform 3. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n), Parallel Enable Input ($\overline{PE}$), and Synchronous Reset Input ($\overline{SR}$).



Waveform 4. Waveforms Showing CEP and CET Set-up and Hold Times

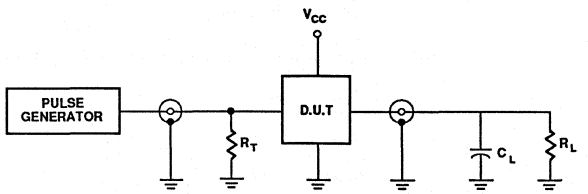
Synchronous presettable BCD decade counter, synchronous reset

74AC/ACT11162

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	May 8, 1990
Status	Preliminary Specification
ACL Products	

74AC/ACT11163

Synchronous presettable 4-bit binary counter, synchronous reset

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Synchronous reset
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11163 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11163 4-bit synchronous presettable binary counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP_n to Q_n ($\overline{PE}$ = High)	C_L = 50pF	5.4	5.9	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	52	51	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	170	155	MHz

Note:

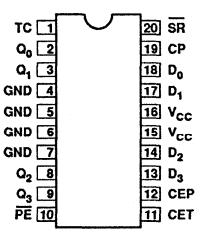
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

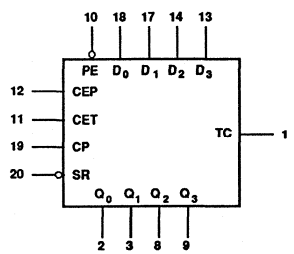
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11163N 74ACT11163N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11163D 74ACT11163D

PIN CONFIGURATION

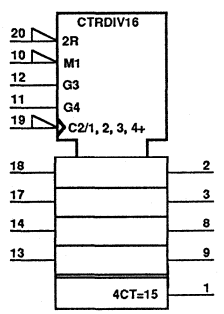
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Synchronous presettable 4-bit binary counter, synchronous reset

74AC/ACT11163

The outputs of the counters may be preset to High or Low levels. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the rising edge of the clock. Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels after the next positive-going transition on the clock (CP) input. This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate.

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the Terminal Count (TC) output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{SR}$	Synchronous reset (active Low)
19	CP	Clock input (Low-to-High edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
12	CEP	Count enable input
10	$\overline{PE}$	Parallel enable input (active Low)
11	CET	Count enable carry input
2, 3, 8, 9	Q_0 - Q_3	Counter outputs
1	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	(1)
Count	h	↑	h	h	h	X	count	(1)
Hold (do nothing)	h	X	l	X	h	X	q_n	(1)
	h	X	X	l	h	X	q_n	L

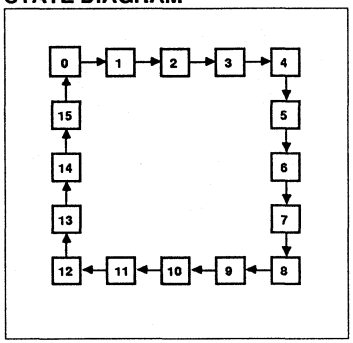
H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to High clock transition
↑ = Low-to-High clock transition

NOTE:
1. The TC output is High when CET is High and the counter is at Terminal Count (HHHH).

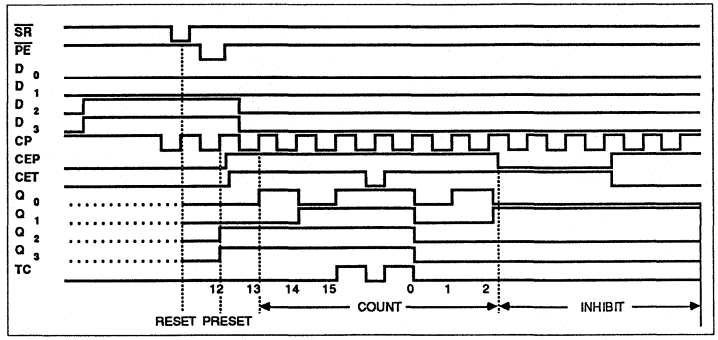
Synchronous presettable 4-bit binary counter, synchronous reset

74AC/ACT11163

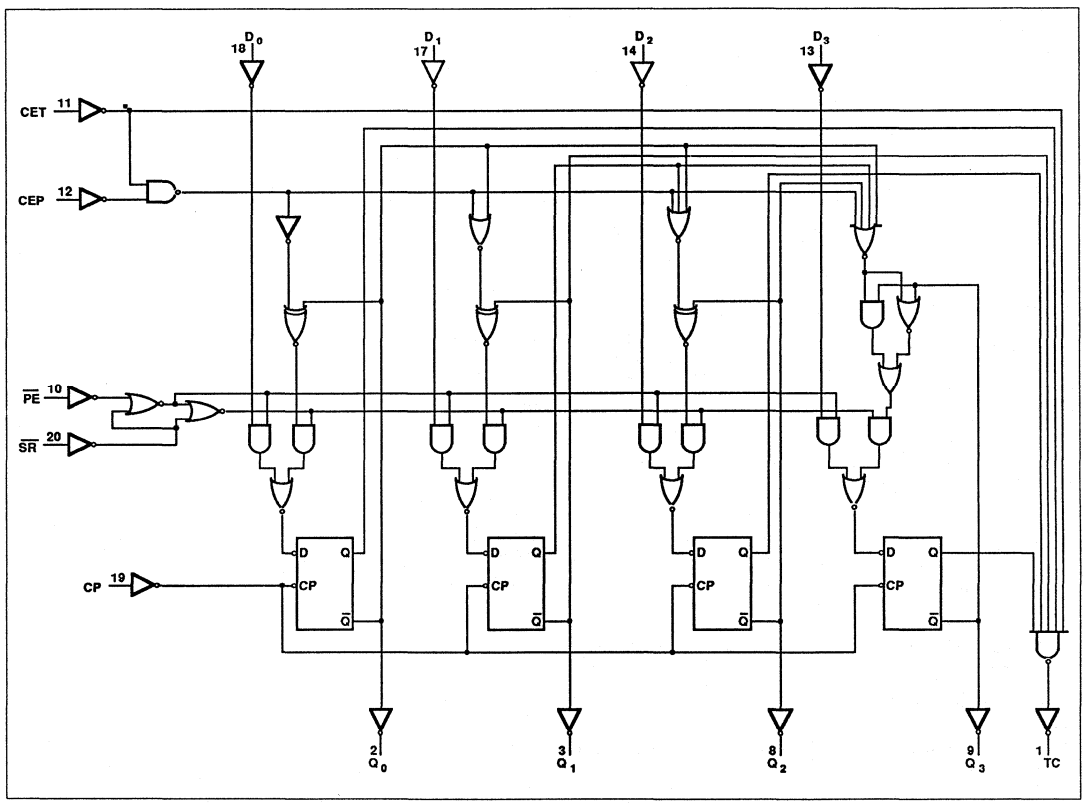
STATE DIAGRAM



TIMING DIAGRAM



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	AC11163			ACT11163			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Synchronous presettable 4-bit binary counter, synchronous reset

74AC/ACT11163

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11163				74ACT11163				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Synchronous presettable 4-bit binary counter, synchronous reset

74AC/ACT11163

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11163					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	90	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	2.5 2.9	7.9 8.6	10.5 11.0	2.5 2.9	11.7 12.3	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	2.6 2.9	7.7 8.4	10.2 10.8	2.6 2.9	11.4 12.1	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	4.0 4.8	10.2 11.3	13.7 13.8	4.0 4.8	15.1 15.5	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	2	1.8 2.3	5.7 6.0	7.5 7.7	1.8 2.3	8.2 8.5	ns
t_S	Setup time, High or Low D_n to CP	3	5.0			5.0		ns
t_H	Hold time, High or Low D_n to CP	3	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	3	6.5			6.5		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	3	0.0			0.0		ns
t_S	Setup time, High or Low CEP or CET to CP	4	6.0			6.0		ns
t_H	Hold time, High or Low CEP or CET to CP	4	0.0			0.0		ns
t_W	Clock pulse width (load) High or Low	1	5.6			5.6		ns
t_W	Clock pulse width (count) High or Low	1	4.0			4.0		ns
t_S	Setup time, High or Low $\overline{SR}$ to CP	3	6.0			6.0		ns
t_H	Hold time, High or Low $\overline{SR}$ to CP	3	0.0			0.0		ns

Synchronous presettable 4-bit binary counter, synchronous reset

74AC/ACT11163

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11163					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	170		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.9 2.3	5.0 5.7	7.3 8.1	1.9 2.3	8.1 9.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.9 2.4	4.8 5.5	7.1 7.9	1.9 2.4	7.8 8.9	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	3.2 4.0	7.2 7.4	9.7 10.3	3.2 4.0	10.6 11.6	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	2	1.4 1.9	3.5 4.3	5.3 6.0	1.4 1.9	5.8 6.6	ns
t_S	Setup time, High or Low D_n to CP	3	3.5			3.5		ns
t_H	Hold time, High or Low D_n to CP	3	0.5			0.5		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	3	4.5			4.5		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	3	0.0			0.0		ns
t_S	Setup time, High or Low CEP or CET to CP	4	4.0			4.0		ns
t_H	Hold time, High or Low CEP or CET to CP	4	0.5			0.5		ns
t_W	Clock pulse width (load) High or Low	1	4.0			4.0		ns
t_W	Clock pulse width (count) High or Low	1	4.0			4.0		ns
t_S	Setup time, High or Low $\overline{SR}$ to CP	3	4.5			4.5		ns
t_H	Hold time, High or Low $\overline{SR}$ to CP	3	0.0			0.0		ns

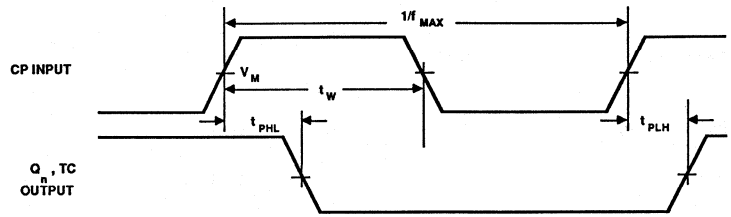
Synchronous presettable 4-bit binary counter, synchronous reset

74AC/ACT11163

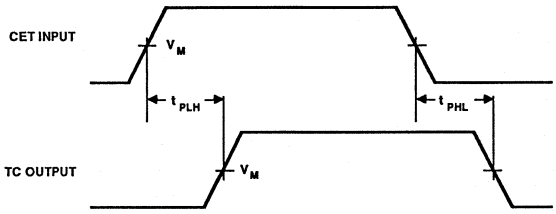
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11163					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	120	155		120		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	2.8 3.2	5.5 6.2	7.6 8.5	2.8 3.2	8.4 9.4	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	2.7 3.2	5.4 6.1	7.3 8.3	2.7 3.2	8.1 9.3	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	3.6 4.6	6.5 7.8	8.6 10.3	3.6 4.6	9.6 11.6	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	2	2.0 3.0	3.9 6.2	5.4 9.1	2.0 3.0	6.0 10.1	ns
t_S	Setup time, High or Low D_n to CP	3	5.0			5.0		ns
t_H	Hold time, High or Low D_n to CP	3	0.5			0.5		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	3	6.0			6.0		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	3	0.5			0.5		ns
t_S	Setup time, High or Low CEP or CET to CP	4	6.5			6.5		ns
t_H	Hold time, High or Low CEP or CET to CP	4	0.5			0.5		ns
t_W	Clock pulse width (load) High or Low	1	4.2			4.2		ns
t_W	Clock pulse width (count) High or Low	1	4.0			4.0		ns
t_S	Setup time, High or Low $\overline{SR}$ to CP	3	7.0			7.0		ns
t_H	Hold time, High or Low $\overline{SR}$ to CP	3	0.5			0.5		ns

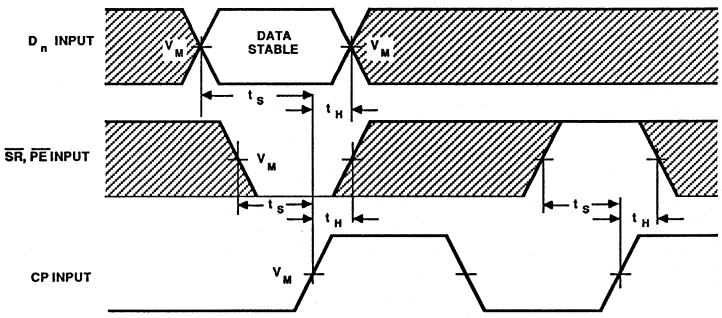
AC WAVEFORMS



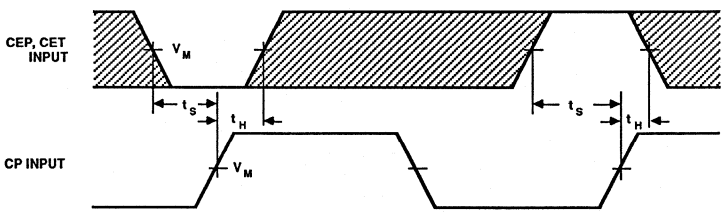
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays, and Clock Pulse Width



Waveform 2. Waveforms Showing the Input (CET) to Output (TC) Propagation Delays



Waveform 3. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n), Parallel Enable Input ($\overline{PE}$), and Synchronous Reset Input ($\overline{SR}$).



Waveform 4. Waveforms Showing CEP and CET Set-up and Hold Times

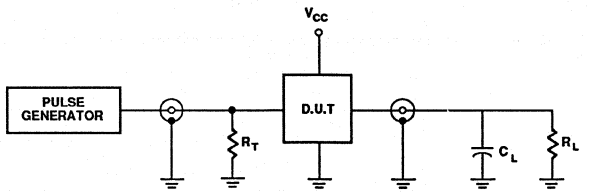
Synchronous presettable 4-bit binary counter, synchronous reset

74AC/ACT11163

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11174

Hex D-type flip-flop with reset, positive-edge trigger

FEATURES

- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11174 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11174 provides six D-type flip-flops with independent Data inputs, shared Clock and Master Reset inputs, and Q outputs.

Master Reset ($\overline{MR}$) is an asynchronous active-Low input and operates independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering is threshold voltage dependent. The D inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF	5.6	6.5	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	29	30	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50 pF	125	135	MHz

Note:

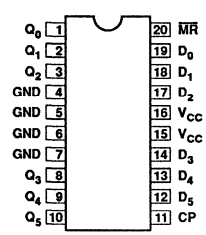
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

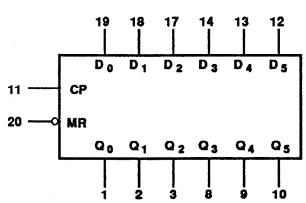
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11174N 74ACT11174N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11174D 74ACT11174D

PIN CONFIGURATION

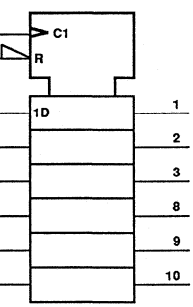
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Hex D-type flip-flop with reset, positive-edge trigger

74AC/ACT11174

PIN DESCRIPTION

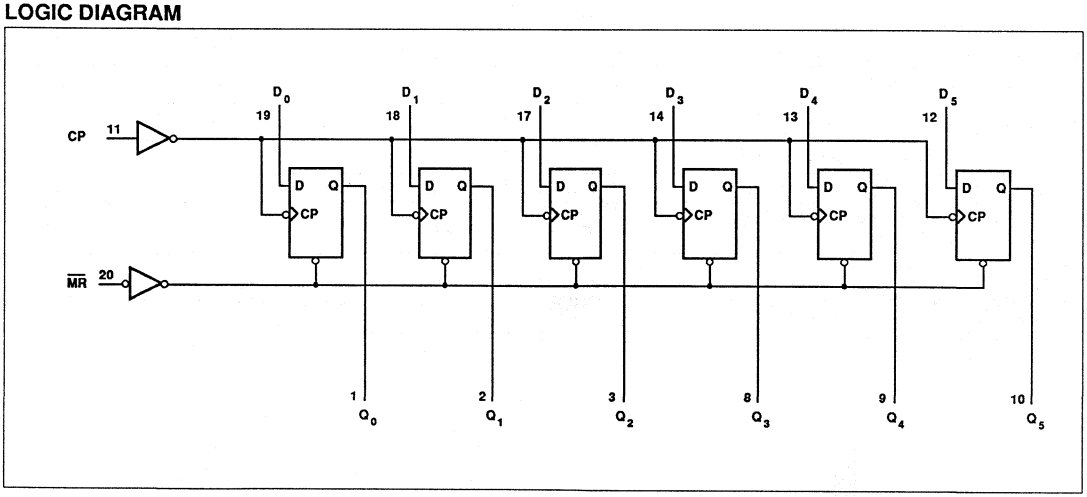
PIN NUMBER	SYMBOL	NAME AND FUNCTION
19, 18, 17, 14, 13, 12	D_0 - D_5	Data inputs
1, 2, 3, 8, 9, 10	Q_0 - Q_5	Data outputs
20	$\overline{MR}$	Master reset input (active Low)
11	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Asynchronous reset	L	X	X	L
Load "1" (set)	H	↑	h	H
Load "0" (reset)	H	↑	l	L

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



Hex D-type flip-flop with reset, positive-edge trigger

74AC/ACT11174

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11174			74ACT11174			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Hex D-type flip-flop with reset, positive-edge trigger

74AC/ACT11174

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11174				74ACT11174				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Hex D-type flip-flop with reset, positive-edge trigger

74AC/ACT11174

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11174					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	80	105		80		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	2.4 3.4	7.5 9.6	9.2 12.7	2.4 3.4	10.6 14.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	3.9	10.0	13.5	3.9	14.8	ns
t_S	Setup time, High or Low D_n to CP	1	7.0			7.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_W	Clock pulse width High or Low	1	6.0			6.0		ns
t_W	$\overline{MR}$ pulse width Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.5			1.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11174					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	2.1 2.7	4.9 6.2	6.8 9.2	2.1 2.7	7.6 10.1	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	2.9	6.5	9.8	2.9	10.7	ns
t_S	Setup time, High or Low D_n to CP	1	4.5			4.5		ns
t_H	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.5			1.5		ns

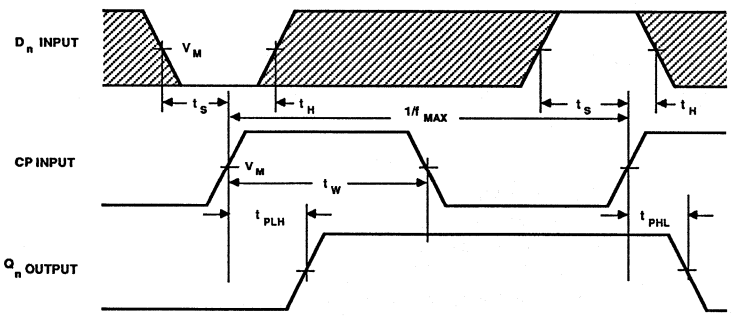
Hex D-type flip-flop with reset, positive-edge trigger

74AC/ACT11174

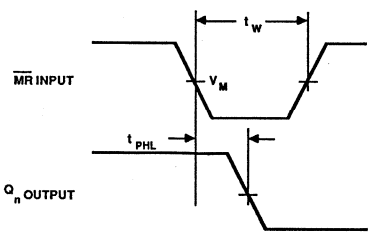
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11174					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	135		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	3.1 3.7	5.8 7.2	7.9 9.9	3.1 3.7	8.7 11.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	3.4	7.5	11.4	3.4	12.6	ns
t_S	Setup time, High or Low D_n to CP	1	4.0			4.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.5			0.5		ns
t_W	Clock pulse width High or Low	1	4.5			4.5		ns
t_W	$\overline{MR}$ pulse width Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.0			1.0		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing Clock to Output Delays, Data Setup, and Clock Pulse Width

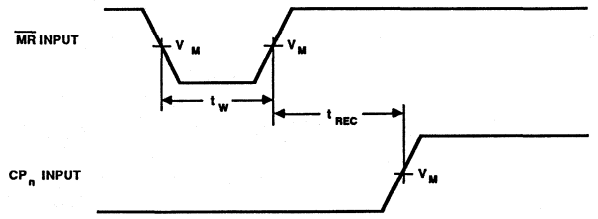


Waveform 2. Waveforms Showing Reset to Output Delay and Reset Pulse Width

Hex D-type flip-flop with reset, positive-edge trigger

74AC/ACT11174

AC WAVEFORMS (Continued)

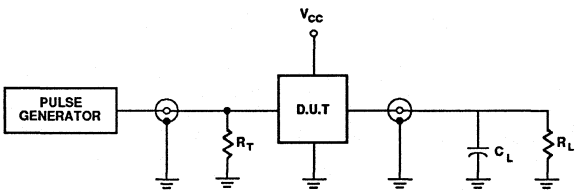


Waveform 3. Waveforms Showing Recovery Time

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11175

Quad D-type flip-flop with reset, positive-edge trigger

FEATURES

- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11175 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11175 provides four D-type flip-flops with independent Data inputs , shared Clock and Master Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Master Reset ($\overline{MR}$) is an asynchronous active-Low input and operates independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering is threshold voltage dependent. The D inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	C_L = 50pF	5.5	6.3	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	47	42	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	150	130	MHz

Note:

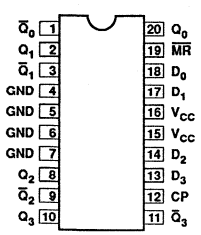
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

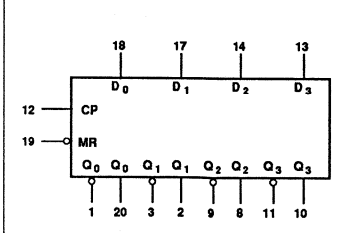
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11175N 74ACT11175N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11175D 74ACT11175D

PIN CONFIGURATION

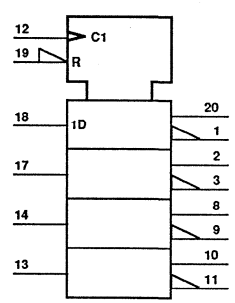
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Quad D-type flip-flop with reset, positive-edge trigger

74AC/ACT11175

PIN DESCRIPTION

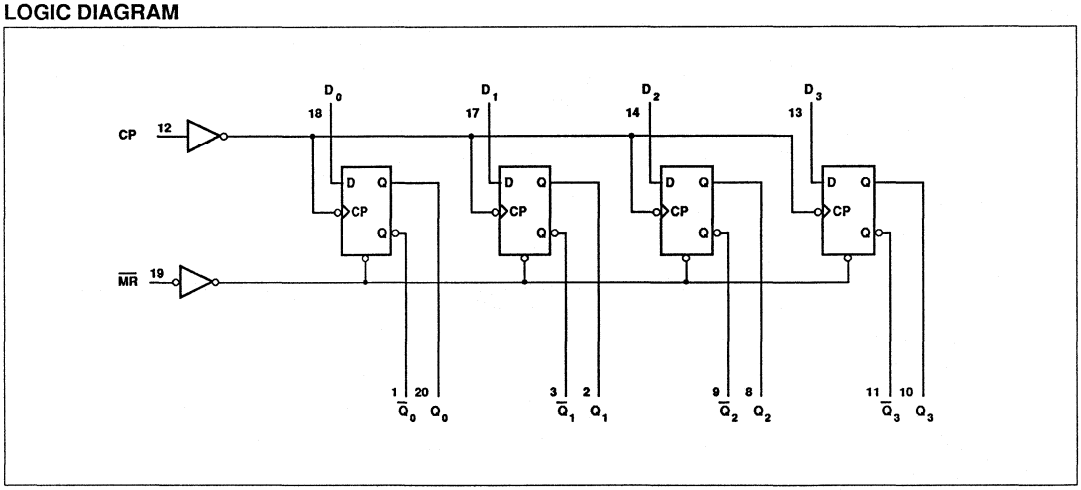
PIN NUMBER	SYMBOL	NAME AND FUNCTION
18, 17, 14, 13	D_0 - D_3	Data inputs
20, 2, 8, 10	Q_0 - Q_3	Data outputs
1, 3, 9, 11	$\overline{Q}_0$ - $\overline{Q}_3$	Data outputs (complements of Q_n outputs)
19	$\overline{MR}$	Master reset input (active Low)
12	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Asynchronous reset	L	X	X	L	H
Load "1" (set)	H	↑	h	H	L
Load "0" (reset)	H	↑	l	L	H

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



Quad D-type flip-flop with reset, positive-edge trigger

74AC/ACT11175

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11175			74ACT11175			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Quad D-type flip-flop with reset, positive-edge trigger

74AC/ACT11175

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11175				74ACT11175				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Quad D-type flip-flop with reset, positive-edge trigger

74AC/ACT11175

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11175					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	90	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	2.4 1.7	6.8 9.4	8.7 11.7	2.4 1.7	9.4 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	2	2.6 2.5	7.0 10.0	8.7 11.6	2.6 2.5	9.3 12.4	ns
t_S	Setup time, High or Low D_n to CP	1	8.0			8.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.5			0.5		ns
t_W	Clock pulse width High or Low	1	5.5			5.5		ns
t_W	$\overline{MR}$ pulse width Low	2	3.5			3.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11175					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	150		125		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	2.2 1.9	4.5 6.4	6.3 8.5	2.2 1.8	6.9 9.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	2	2.2 2.4	4.5 6.7	6.3 8.5	2.2 2.4	6.8 9.3	ns
t_S	Setup time, High or Low D_n to CP	1	5.5			5.5		ns
t_H	Hold time, High or Low CP to D_n	1	0.5			0.5		ns
t_W	Clock pulse width High or Low	1	4.0			4.0		ns
t_W	$\overline{MR}$ pulse width Low	2	2.5			2.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.0			1.0		ns

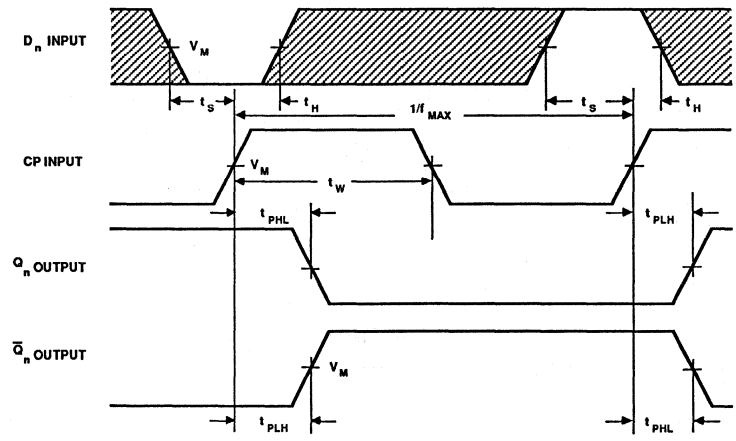
Quad D-type flip-flop with reset, positive-edge trigger

74AC/ACT11175

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

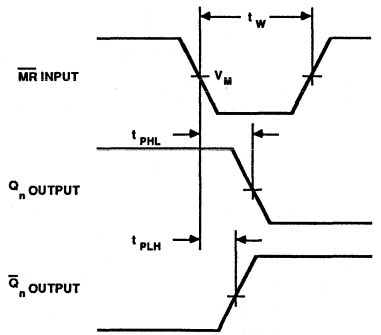
SYMBOL	PARAMETER	WAVEFORM	74ACT11175					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	3.0 3.3	5.3 7.2	6.9 9.2	3.0 3.3	7.5 10.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	2	2.5 3.1	5.4 7.6	7.4 9.9	2.5 3.1	8.1 10.9	ns
t_S	Setup time, High or Low D_n to CP	1	5.0			5.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.5			0.5		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.5			1.5		ns

AC WAVEFORMS

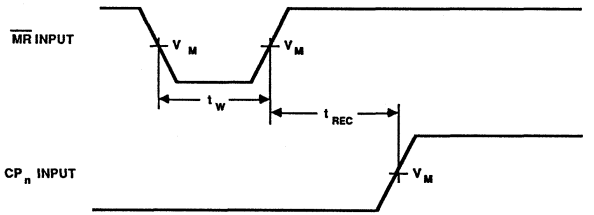


Waveform 1. Waveforms Showing Clock to Output Delays, Data Setup, and Clock Pulse Width

AC WAVEFORMS (Continued)



Waveform 2. Waveforms Showing Master Reset to Output Delay and Master Reset Pulse Width

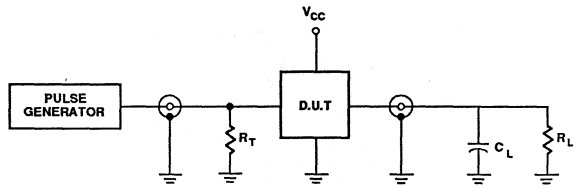


Waveform 3. Waveforms Showing Recovery Time

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

Date of Issue	June 12, 1990
Status	Preliminary Specification
ACL Products	

74AC/ACT11181

4-bit arithmetic logic unit

FEATURES

- Provides 16 arithmetic operations: add, subtract, compare, and double; plus 12 other arithmetic operations
- Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations
- Full look-ahead Carry for high-speed arithmetic operation on long words
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11181 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11181 arithmetic logic units (ALU) are controlled by the four Function Select inputs (S_0 - S_3) and the Mode Control input (M) and can perform all the 16 possible logic operations or 16 different arithmetic operations on active-High or active-Low operands. The Function Tables list these operations.

When the Mode Control input (M) is High, all internal carries are inhibited and the device performs logic opera-

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$ (sum mode)	C_L = 50pF	9.5	11.6	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	119	119	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC} (A = B)	11	11	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

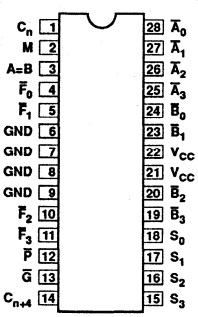
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

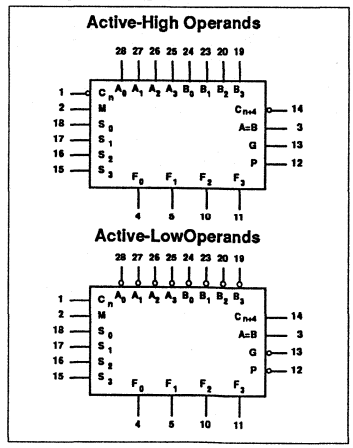
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11181N 74ACT11181N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11181D 74ACT11181D

PIN CONFIGURATION

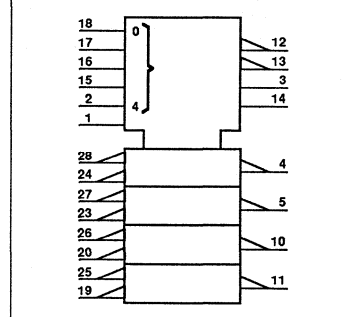
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



4-bit arithmetic logic unit 74AC/ACT11181

tions on the individual bits as listed. When the Mode Control input is Low, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry look-ahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with the 74AC/ACT11882 carry look-ahead circuit. One carry look-ahead package is required for each group of eight 74AC/ACT11181 devices. Carry look-ahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes High when all four $\overline{F}$ outputs are High and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with other A = B outputs to give a comparison for more than 4 bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Tables list both the arithmetic operations that are performed without a carry in and with a carry in. Note that a carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (two's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (one's complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active-Low inputs producing active-Low outputs or with active-High inputs producing active-High outputs. For either case, the tables list the operations that are performed to the operands labeled inside the logic symbol.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2	M	Mode control input
28, 27, 26, 25	$\overline{A}_0$ - $\overline{A}_3$	$\overline{A}$ operand inputs
24, 23, 20, 19	$\overline{B}_0$ - $\overline{B}_3$	$\overline{B}$ operand inputs
18, 17, 16, 15	S_0 - S_3	Function select inputs
1	C_n	Carry input
14	C_{n+4}	Carry output
3	A = B	Compare output
4, 5, 10, 11	$\overline{F}_0$ - $\overline{F}_3$	Outputs
13	$\overline{G}$	Carry generate output
12	$\overline{P}$	Carry propagate output
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

The 74AC/ACT11181 devices will accomdate active-High or active-Low data if the pin designations are interpreted as follows:

PIN NUMBER	28	24	27	23	26	20	25	19	4	5	10	11	1	14	12	13
Active-Low data (Table 1)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_0$	$\overline{F}_0$	$\overline{F}_0$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-High data (Table 2)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_0	F_0	F_0	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

FUNCTION TABLE FOR ACTIVE-LOW DATA

SELECTION				ACTIVE LOW INPUTS & OUTPUTS		
				LOGIC (M = H)	ARITHMETIC** (M = L)	
S3	S2	S1	S0		C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$\overline{A}$	A minus 1	A
L	L	L	H	$\overline{AB}$	AB minus 1	AB
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1	$A\overline{B}$
L	L	H	H	Logical 1	minus 1	0 (zero)
L	H	L	L	$\overline{A+B}$	A plus $(A+\overline{B})$	A plus $(A+\overline{B})$ plus 1
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$	AB plus $(A+\overline{B})$ plus 1
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A minus B
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	$(A+\overline{B})$ plus 1
H	L	L	L	$\overline{AB}$	A plus (A + B)	A plus (A + B) plus 1
H	L	L	H	$A \oplus B$	A plus B	A plus B plus 1
H	L	H	L	B	$A\overline{B}$ plus (A + B)	$A\overline{B}$ plus (A + B) plus 1
H	L	H	H	A + B	(A + B)	(A + B) plus 1
H	H	L	L	Logical 0	A plus A*	A plus A plus 1
H	H	L	H	$A\overline{B}$	AB plus A	AB plus A plus 1
H	H	H	L	AB	A plus $A\overline{B}$	A plus $A\overline{B}$ plus 1
H	H	H	H	A	A	A plus 1

L = Low voltage
H = High voltage level
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in two's complement notation.

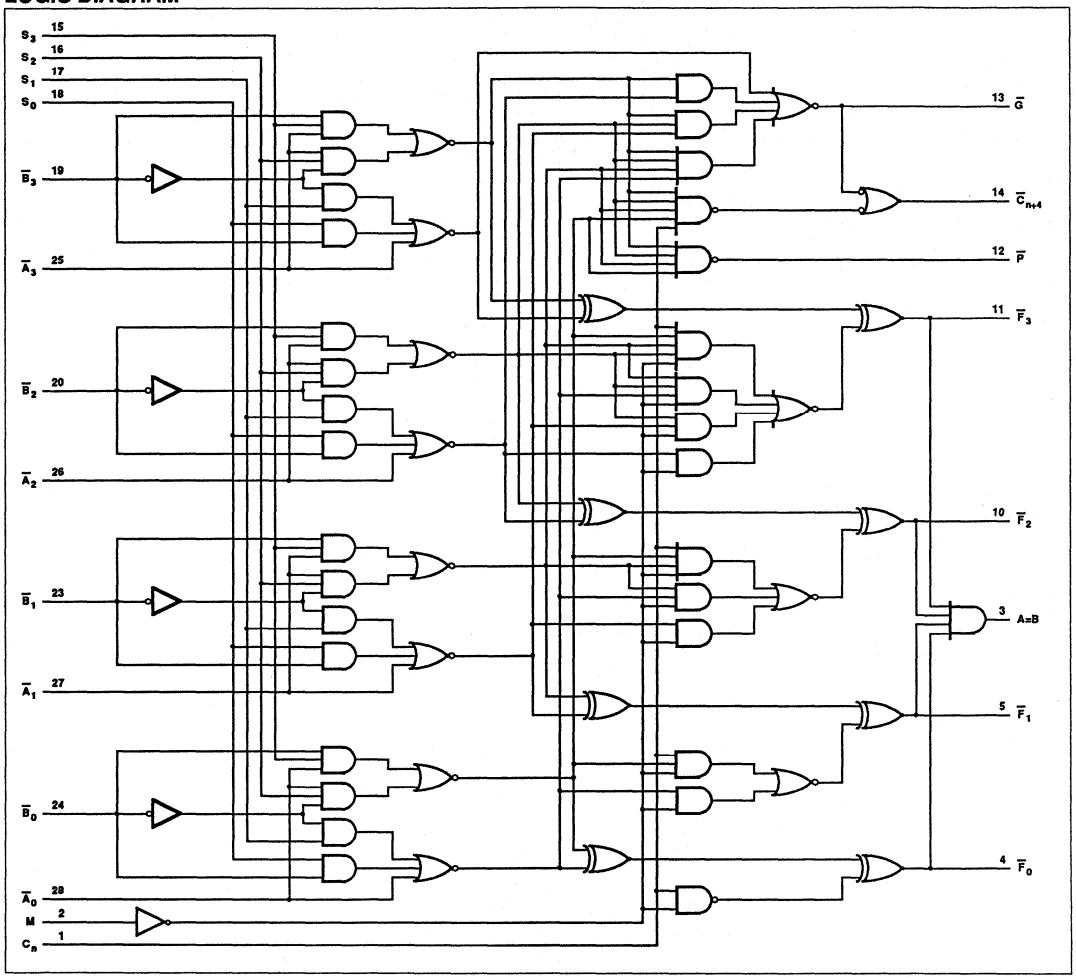
FUNCTION TABLE FOR ACTIVE-HIGH DATA

SELECTION				ACTIVE HIGH INPUTS & OUTPUTS		
				LOGIC (M = H)	ARITHMETIC** (M = L)	
S3	S2	S1	S0		C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	$\overline{A}$	A	A plus 1
L	L	L	H	$\overline{A+B}$	(A + B)	$(A+\overline{B})$ plus 1
L	L	H	L	$\overline{AB}$	$A+\overline{B}$	$(A+\overline{B})$ plus 1
L	L	H	H	Logical 0	minus 1	0 (zero)
L	H	L	L	$\overline{AB}$	A plus $A\overline{B}$	A plus $A\overline{B}$ plus 1
L	H	L	H	$\overline{B}$	$A\overline{B}$ plus (A + B)	$A\overline{B}$ plus (A + B) plus 1
L	H	H	L	$A \oplus B$	A minus B minus 1	A minus B
L	H	H	H	$A\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
H	L	L	L	$\overline{A}+B$	AB plus A	AB plus A plus 1
H	L	L	H	$\overline{A \oplus B}$	A plus B	A plus B plus 1
H	L	H	L	B	AB plus $(A+\overline{B})$	AB plus $(A+\overline{B})$ plus 1
H	L	H	H	AB	AB minus 1	AB
H	H	L	L	Logical 1	A plus A*	A plus A plus 1
H	H	L	H	$A+\overline{B}$	A plus (A + B)	A plus (A + B) plus 1
H	H	H	L	A + B	A plus $(A+\overline{B})$	A plus $(A+\overline{B})$ plus 1
H	H	H	H	A	A minus 1	A

L = Low voltage
H = High voltage level
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in two's complement notation.

4-bit arithmetic logic unit 74AC/ACT11181

LOGIC DIAGRAM



SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0 = S_3 = V_{CC}$, $S_1 = S_2 = M = GND$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	WAVEFORM
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	1
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	1
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	1
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining C_n	$\overline{G}$	1
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	2
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	2
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	1

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_1 = S_2 = V_{CC}$, $S_0 = S_3 = M = GND$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	WAVEFORM
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	1
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	2
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	2
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	1
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	2
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	1
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	2
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	2
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	1
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}	1

LOGIC MODE TEST TABLE III **FUNCTION INPUTS:** $S_1 = S_2 = M = V_{CC}$, $S_0 = S_3 = GND$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	WAVEFORM
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	2
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	2

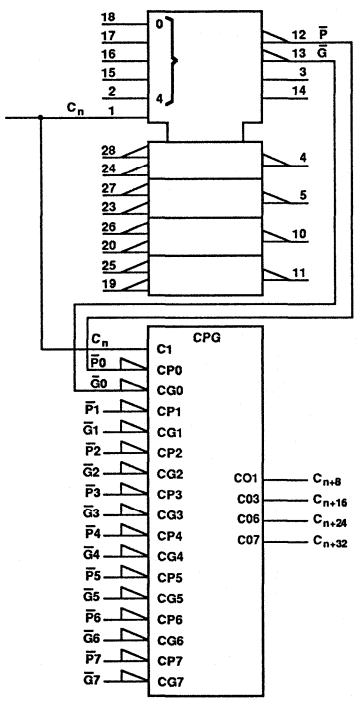


Figure 1

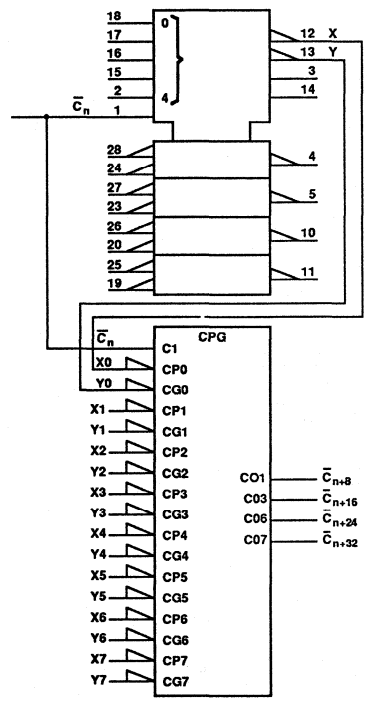


Figure 2

The signal designations in Figure 1 agree with the indicated internal functions based on active-Low data and are for use with the logic functions and arithmetic operations shown in the Function Table for Active-Low Data. The signal designators have been changed in Figure 2 to accommodate the logic functions and arithmetic operations given in the Function Table for Active-High Data.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11181			74ACT11181			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS			74AC11181				74ACT11181				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
I_{OH}	High-level output current	A = B; V_O = V_{CC}		5.5		0.5		5.0		0.5		5.0	µA
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage (any output except A=B)	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	µA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V—SUM MODE; M = S_1 = S_2 = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	74AC11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$		1.5 1.5	10.5 8.1	14.9 11.6	1.5 1.5	15.6 15.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	S_0 = S_3 = 4.5V	1.5 1.5	13.0 13.7	18.5 17.7	1.5 1.5	19.7 20.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	S_0 = S_3 = 4.5V	1.5 1.5	14.4 13.5	19.4 17.6	1.5 1.5	21.2 19.8	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	M = 0V	1.5 1.5	13.2 10.7	21.0 16.5	1.5 1.5	22.4 17.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	S_0 = S_3 = 4.5V	1.5 1.5	14.2 10.9	19.6 14.5	1.5 1.5	21.3 18.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	S_0 = S_3 = 4.5V	1.5 1.5	13.8 11.8	19.2 14.7	1.5 1.5	20.8 17.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	S_0 = S_3 = 4.5V	1.5 1.5	12.6 9.8	15.9 12.3	1.5 1.5	17.6 13.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	S_0 = S_3 = 4.5V	1.5 1.5	12.4 10.2	15.7 13.2	1.5 1.5	17.2 14.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	S_0 = S_3 = 4.5V	1.5 1.5	14.4 11.8	18.4 14.6	1.5 1.5	19.7 16.2	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	S_0 = S_3 = 4.5V	1.5 1.5	13.7 12.7	17.7 15.4	1.5 1.5	19.4 17.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	S_0 = S_3 = 4.5V	1.5 1.5	16.2 13.9	21.7 18.4	1.5 1.5	23.7 20.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	S_0 = S_3 = 4.5V	1.5 1.5	16.0 14.4	21.5 19.1	1.5 1.5	23.6 21.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	S_0 = S_3 = 4.5V	1.5 1.5	10.3 9.2	13.2 11.2	1.5 1.5	14.5 12.2	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	S_0 = S_3 = 4.5V	1.5 1.5	16.6 12.2	20.7 14.8	1.5 1.5	21.6 17.1	ns

NOTE: "$\overline{A}_n$ to $\overline{F}_n$" means any $\overline{A}$ to any $\overline{F}$ while "$\overline{A}_i$ to $\overline{F}_i$" means $\overline{A}_1$ to $\overline{F}_1$; $\overline{A}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V—DIFF MODE; M = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	74AC11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}		1.5 1.5	10.5 8.1	14.9 11.6	1.5 1.5	15.6 15.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to C_{n+4}	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	13.5 13.6	18.7 17.9	1.5 1.5	19.9 20.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to C_{n+4}	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	15.4 14.0	20.3 18.3	1.5 1.5	21.8 20.4	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$	M = 0V	1.5 1.5	13.2 10.7	21.0 16.5	1.5 1.5	22.4 17.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{G}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	14.1 10.8	19.7 14.6	1.5 1.5	21.3 17.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{G}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	14.5 12.4	20.0 15.7	1.5 1.5	21.3 18.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{P}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	12.8 9.9	16.4 12.5	1.5 1.5	18.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{P}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	13.1 11.2	16.4 14.1	1.5 1.5	17.9 15.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	14.7 11.9	18.9 14.9	1.5 1.5	20.1 16.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	14.5 13.5	18.3 16.2	1.5 1.5	19.9 18.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{F}_n$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	16.4 14.1	22.0 18.8	1.5 1.5	24.0 20.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{F}_n$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	16.5 15.3	22.2 19.8	1.5 1.5	24.2 21.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to A=B	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	20.6 15.0	25.1 18.2	1.5 1.5	27.5 21.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to A=B	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	20.4 16.7	25.0 19.7	1.5 1.5	27.0 22.1	ns

NOTE: "$\overline{A}_n$ to $\overline{F}_n$" means any $\overline{A}$ to any $\overline{F}$ while "$\overline{A}_i$ to $\overline{F}_i$" means $\overline{A}_1$ to $\overline{F}_1$; $\overline{A}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V—LOGIC AND $\overline{ARITH}$ MODE

SYMBOL	PARAMETER	TEST CONDITIONS	74AC11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	M = 4.5V (LOGIC mode)	1.5 1.5	11.5 12.2	15.2 15.0	1.5 1.5	16.6 16.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	M = 4.5V (LOGIC mode)	1.5 1.5	14.7 13.3	18.9 16.5	1.5 1.5	20.4 18.2	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	16.1 12.5	20.5 15.1	1.5 1.5	21.2 17.3	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	22.8 16.0	27.1 19.0	1.5 1.5	29.5 21.2	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	M = 4.5V (LOGIC mode)	1.5 1.5	14.9 17.0	20.3 24.0	1.5 1.5	21.4 26.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	15.7 12.6	21.6 17.8	1.5 1.5	23.6 21.3	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	M = 4.5V (LOGIC mode)	1.5 1.5	16.7 12.0	20.0 15.5	1.5 1.5	22.4 17.6	ns

NOTE: "$\overline{B}_n$ to $\overline{F}_n$" means any $\overline{B}$ to any $\overline{F}$ while "$\overline{B}_i$ to $\overline{F}_i$" means $\overline{B}_1$ to $\overline{F}_1$; $\overline{B}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V—SUM MODE; $M = S_1 = S_2 = 0V$

SYMBOL	PARAMETER	TEST CONDITIONS	74AC11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$		1.5 1.5	7.1 7.5	9.9 11.4	1.5 1.5	10.8 14.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	$S_0 = S_3 = 4.5V$	1.5 1.5	9.6 10.0	14.3 17.2	1.5 1.5	14.5 18.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	$S_0 = S_3 = 4.5V$	1.5 1.5	9.6 10.6	14.8 17.0	1.5 1.5	15.2 18.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	M = 0V	1.5 1.5	9.2 8.3	14.0 13.1	1.5 1.5	14.9 14.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	$S_0 = S_3 = 4.5V$	1.5 1.5	9.2 8.3	13.2 14.3	1.5 1.5	14.6 16.3	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	$S_0 = S_3 = 4.5V$	1.5 1.5	9.1 8.8	13.0 13.6	1.5 1.5	14.4 16.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	$S_0 = S_3 = 4.5V$	1.5 1.5	8.4 7.7	13.3 10.7	1.5 1.5	14.1 11.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	$S_0 = S_3 = 4.5V$	1.5 1.5	7.9 8.3	13.0 10.7	1.5 1.5	13.8 11.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	$S_0 = S_3 = 4.5V$	1.5 1.5	9.5 9.4	14.3 14.6	1.5 1.5	15.5 15.9	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	$S_0 = S_3 = 4.5V$	1.5 1.5	9.2 10.0	14.0 15.3	1.5 1.5	15.2 16.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	$S_0 = S_3 = 4.5V$	1.5 1.5	10.8 10.3	14.1 15.3	1.5 1.5	15.4 16.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	$S_0 = S_3 = 4.5V$	1.5 1.5	10.4 10.7	14.1 15.6	1.5 1.5	15.3 17.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	$S_0 = S_3 = 4.5V$	1.5 1.5	7.3 8.3	9.2 11.2	1.5 1.5	9.9 12.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	$S_0 = S_3 = 4.5V$	1.5 1.5	14.3 11.7	17.7 14.8	1.5 1.5	18.5 17.1	ns

NOTE: "$\overline{A}_n$ to $\overline{F}_n$" means any $\overline{A}$ to any $\overline{F}$ while "$\overline{A}_i$ to $\overline{F}_i$" means $\overline{A}_1$ to $\overline{F}_1$; $\overline{A}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V—DIFF MODE; M = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	74AC11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}		1.5 1.5	7.1 7.5	9.9 11.4	1.5 1.5	10.8 14.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to C_{n+4}	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	9.5 10.5	14.6 17.3	1.5 1.5	14.8 19.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to C_{n+4}	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	10.5 11.3	15.4 17.4	1.5 1.5	16.0 19.0	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$	M = 0V	1.5 1.5	9.2 8.3	14.0 13.1	1.5 1.5	14.9 14.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{G}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	9.1 8.4	13.4 14.6	1.5 1.5	14.7 16.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{G}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	9.6 9.5	13.8 14.2	1.5 1.5	15.0 17.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{P}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	8.7 8.0	13.4 10.2	1.5 1.5	14.2 11.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{P}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	8.6 8.8	13.3 11.3	1.5 1.5	14.1 12.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	9.7 9.7	14.5 14.5	1.5 1.5	15.7 15.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	9.4 10.8	14.4 16.0	1.5 1.5	15.5 17.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{F}_n$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	11.0 10.5	14.3 15.5	1.5 1.5	15.6 16.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{F}_n$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	10.9 11.2	14.3 15.3	1.5 1.5	15.7 17.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to A=B	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	16.5 12.8	20.2 16.4	1.5 1.5	22.7 21.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to A=B	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	16.3 13.6	20.0 18.4	1.5 1.5	22.1 21.2	ns

NOTE: "$\overline{A}_n$ to $\overline{F}_n$" means any $\overline{A}$ to any $\overline{F}$ while "$\overline{A}_i$ to $\overline{F}_i$" means $\overline{A}_1$ to $\overline{F}_1$; $\overline{A}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V—LOGIC AND $\overline{ARITH}$ MODE

SYMBOL	PARAMETER	TEST CONDITIONS	74AC11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	M = 4.5V (LOGIC mode)	1.5 1.5	7.6 9.8	11.7 15.0	1.5 1.5	12.7 16.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	M = 4.5V (LOGIC mode)	1.5 1.5	9.8 10.5	14.5 15.6	1.5 1.5	15.5 17.2	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	10.6 9.8	13.9 12.7	1.5 1.5	15.2 16.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	17.7 12.3	21.4 19.0	1.5 1.5	22.7 20.9	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	M = 4.5V (LOGIC mode)	1.5 1.5	9.9 11.6	14.3 21.0	1.5 1.5	15.4 23.3	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	10.1 9.0	14.4 15.2	1.5 1.5	16.0 18.4	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	M = 4.5V (LOGIC mode)	1.5 1.5	10.8 9.0	14.8 11.5	1.5 1.5	16.4 14.3	ns

NOTE: "$\overline{B}_n$ to $\overline{F}_n$" means any $\overline{B}$ to any $\overline{F}$ while "$\overline{B}_i$ to $\overline{F}_i$" means $\overline{B}_1$ to $\overline{F}_1$; $\overline{B}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V—SUM MODE; $M = S_1 = S_2 = 0V$

SYMBOL	PARAMETER	TEST CONDITIONS	74ACT11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}		1.5 1.5	10.7 11.3	17.5 16.2	1.5 1.5	18.6 18.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to C_{n+4}	$S_0 = S_3 = 4.5V$	1.5 1.5	12.7 14.0	20.3 19.7	1.5 1.5	21.8 22.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to C_{n+4}	$S_0 = S_3 = 4.5V$	1.5 1.5	13.5 13.6	21.6 19.7	1.5 1.5	23.2 22.0	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$	M = 0V	1.5 1.5	11.2 9.9	17.1 15.9	1.5 1.5	18.7 17.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{G}$	$S_0 = S_3 = 4.5V$	1.5 1.5	12.8 12.7	20.9 17.8	1.5 1.5	23.3 20.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{G}$	$S_0 = S_3 = 4.5V$	1.5 1.5	12.7 14.3	20.6 19.2	1.5 1.5	22.1 21.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{P}$	$S_0 = S_3 = 4.5V$	1.5 1.5	11.4 9.6	18.4 16.6	1.5 1.5	19.6 17.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{P}$	$S_0 = S_3 = 4.5V$	1.5 1.5	11.3 10.6	18.2 15.6	1.5 1.5	19.3 16.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	$S_0 = S_3 = 4.5V$	1.5 1.5	11.8 11.0	17.7 17.1	1.5 1.5	19.5 18.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	$S_0 = S_3 = 4.5V$	1.5 1.5	11.6 12.0	17.3 19.4	1.5 1.5	19.1 20.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{F}_n$	$S_0 = S_3 = 4.5V$	1.5 1.5	13.0 12.4	18.9 18.8	1.5 1.5	21.0 20.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{F}_n$	$S_0 = S_3 = 4.5V$	1.5 1.5	13.1 13.5	18.7 19.8	1.5 1.5	21.0 21.3	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_n$	$S_0 = S_3 = 4.5V$	1.5 1.5	9.5 10.6	15.0 16.4	1.5 1.5	16.3 17.5	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B	$S_0 = S_3 = 4.5V$	1.5 1.5	15.7 14.0	19.3 18.7	1.5 1.5	20.1 21.8	ns

NOTE: "$\overline{A}_n$ to $\overline{F}_n$" means any $\overline{A}$ to any $\overline{F}$ while "$\overline{A}_i$ to $\overline{F}_i$" means $\overline{A}_1$ to $\overline{F}_1$; $\overline{A}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V—DIFF MODE; M = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	74ACT11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}		1.5 1.5	10.7 11.0	17.3 16.2	1.5 1.5	18.6 18.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to C_{n+4}	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	12.7 13.5	20.3 19.7	1.5 1.5	21.8 20.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to C_{n+4}	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	13.8 14.8	21.1 20.7	1.5 1.5	22.7 23.0	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$	M = 0V	1.5 1.5	11.2 9.9	17.1 15.9	1.5 1.5	18.7 17.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{G}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	12.8 12.7	20.8 18.4	1.5 1.5	22.2 20.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{G}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	13.2 13.4	20.8 18.7	1.5 1.5	21.6 21.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{P}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	11.5 9.6	18.5 14.6	1.5 1.5	19.6 15.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{P}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	10.8 10.4	18.8 15.1	1.5 1.5	20.0 16.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	11.9 11.2	17.8 17.2	1.5 1.5	19.6 19.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	12.1 12.0	17.8 18.6	1.5 1.5	19.5 20.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{F}_n$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	13.2 12.6	19.0 18.9	1.5 1.5	21.1 20.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{F}_n$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	13.6 13.1	19.4 18.7	1.5 1.5	21.5 20.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to A=B	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	18.0 16.0	21.6 21.5	1.5 1.5	23.7 24.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to A=B	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	18.5 16.5	22.7 22.0	1.5 1.5	23.9 25.4	ns

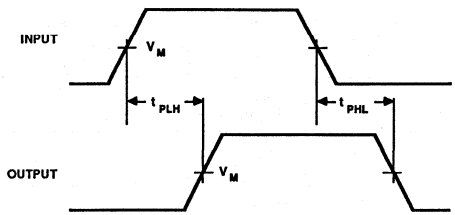
NOTE: "$\overline{A}_n$ to $\overline{F}_n$" means any $\overline{A}$ to any $\overline{F}$ while "$\overline{A}_i$ to $\overline{F}_i$" means $\overline{A}_1$ to $\overline{F}_1$; $\overline{A}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V—LOGIC AND $\overline{ARITH}$ MODE

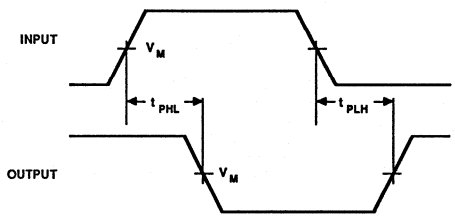
SYMBOL	PARAMETER	TEST CONDITIONS	74ACT11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	M = 4.5V (LOGIC mode)	1.5 1.5	10.0 11.0	15.9 17.4	1.5 1.5	18.3 19.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	M = 4.5V (LOGIC mode)	1.5 1.5	12.2 11.5	18.0 18.3	1.5 1.5	19.6 19.6	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	12.1 10.6	18.3 15.8	1.5 1.5	20.1 17.4	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	18.7 17.2	22.1 22.2	1.5 1.5	23.4 25.4	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	M = 4.5V (LOGIC mode)	1.5 1.5	13.9 15.3	21.8 22.3	1.5 1.5	23.6 25.2	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	12.7 13.5	20.5 19.7	1.5 1.5	22.3 22.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	M = 4.5V (LOGIC mode)	1.5 1.5	12.4 11.7	18.6 17.7	1.5 1.5	20.5 18.0	ns

NOTE: "$\overline{B}_n$ to $\overline{F}_n$" means any $\overline{B}$ to any $\overline{F}$ while "$\overline{B}_i$ to $\overline{F}_i$" means $\overline{B}_1$ to $\overline{F}_1$; $\overline{B}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC WAVEFORMS



Waveform 1. Waveforms Showing Propagation Delays for Non-Inverting Paths

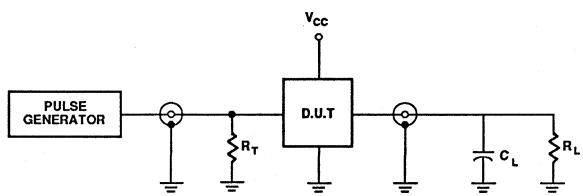


Waveform 2. Waveforms Showing Propagation Delays for Inverting Paths

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11190

Asynchronous presettable synchronous decade up/down counter with single clock

FEATURES

- Synchronous, reversible counting
- Positive edge-triggered clock
- BCD/decade
- Asynchronous Parallel Load capability
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11190 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11190 is an asynchronously presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = High)	C_L = 50pF	5.2	7.3	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	68	70	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency; CP → Q_n	C_L = 50pF	150	120	MHz

Note:

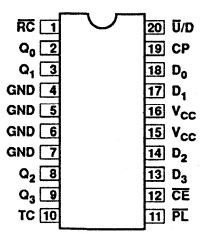
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

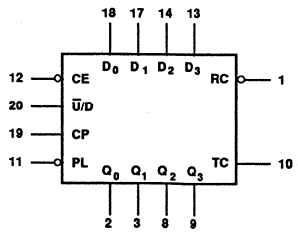
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11190N 74ACT11190N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11190D 74ACT11190D

PIN CONFIGURATION

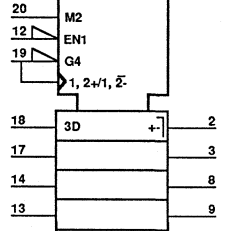
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Asynchronous presettable synchronous decade up/down counter with single clock

74AC/ACT11190

Asynchronous Parallel Load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a High level on the Count Enable ($\overline{CE}$) input.

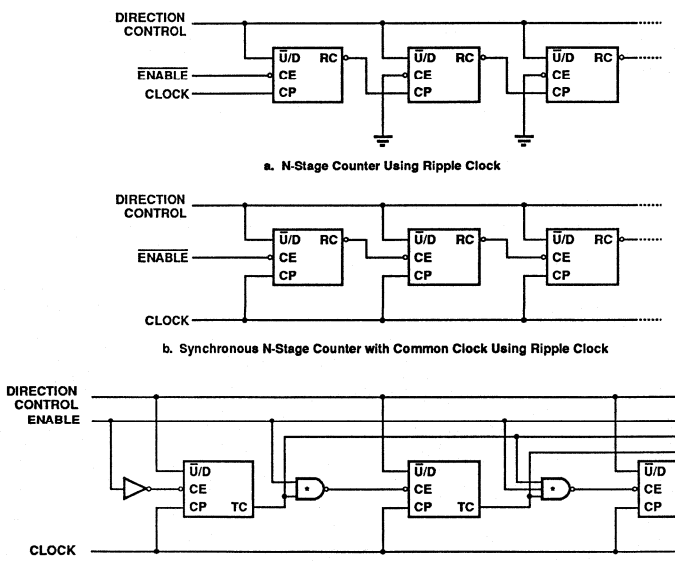
Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally Low and goes High when: 1) the count reaches zero in the count-down mode or 2) reaches "9" in the Count-up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output.

When TC is High and $\overline{CE}$ is Low, the $\overline{RC}$ follows the Clock Pulse. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays. The 74AC/ACT11190 simplifies the design of multistage counters, as indicated in Figures 1a and 1b.

In Figure 1a, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the Clock input source has limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any package goes High shortly after its CP input goes High, there is no such restriction on the High state duration of the clock.

In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.



a. N-Stage Counter Using Ripple Clock

b. Synchronous N-Stage Counter with Common Clock Using Ripple Clock

c. Synchronous N-Stage Counter with Common Clock and Parallel Gated Terminal Count

Figure 1

Asynchronous presettable synchronous decade up/down counter with single clock

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{U}/D$	Up/down count control input
12	$\overline{CE}$	Count enable input (active-Low)
18, 17, 14, 13	D_0 - D_3	Data inputs
19	CP	Clock pulse input (active rising edge)
11	$\overline{PL}$	Asynchronous load input (active-Low)
2, 3, 8, 9	Q_0 - Q_3	Counter outputs
1	$\overline{RC}$	Ripple clock output (active-Low)
10	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold (do nothing)	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	L	L	H	H	H
L	L	⊓	H	L	L	H	H	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	H	⊓

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
↑ = Low-to-High clock transition
⊓ = Low pulse

Asynchronous presettable synchronous decade up/down counter with single clock

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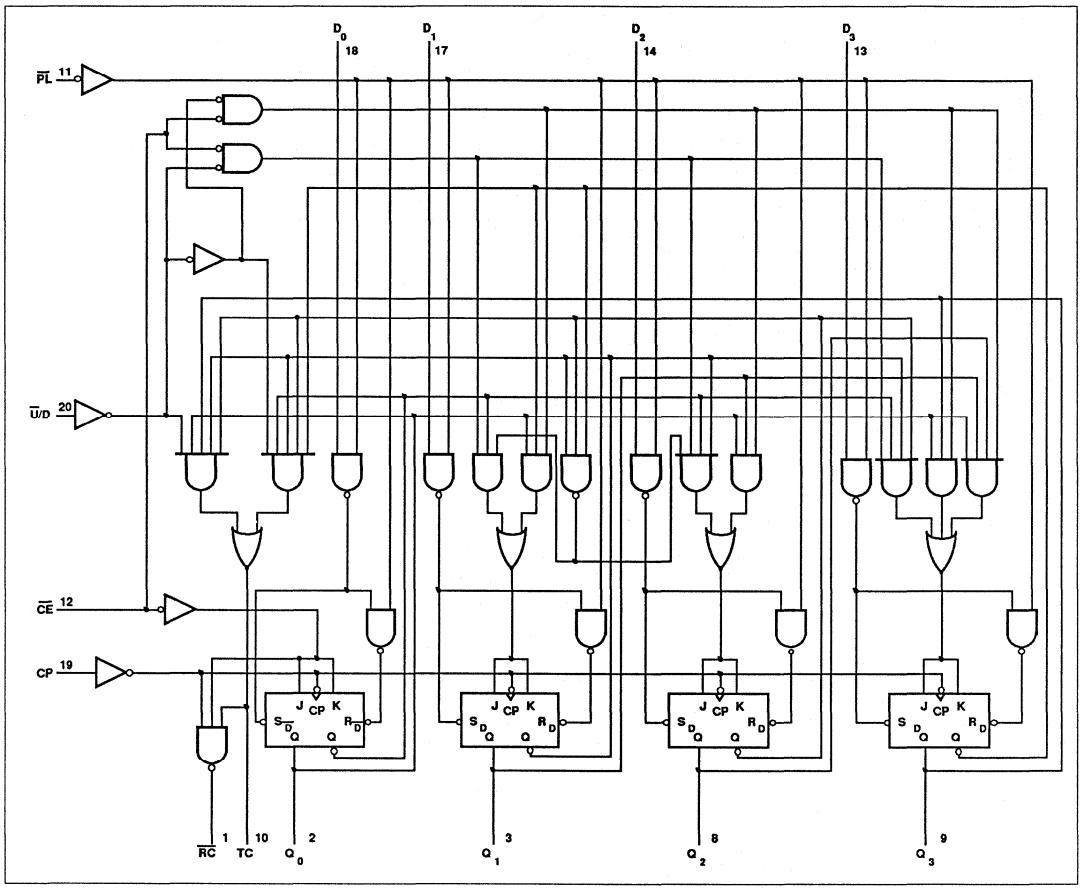
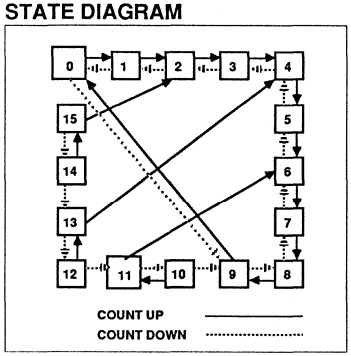
LOGIC DIAGRAM



STATE DIAGRAM



Asynchronous presettable synchronous decade up/down counter with single clock

74AC/ACT11190

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11190			74ACT11190			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Asynchronous presettable synchronous decade up/down counter with single clock

74AC/ACT11190

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11190				74ACT11190				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Asynchronous presettable synchronous decade up/down counter with single clock

74AC/ACT11190

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER		WAVEFORM	74AC11190					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	65	95		65		MHz
		CP to $\overline{RC}$, TC		60	85		60		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	2.3 2.8	7.6 7.2	10.0 9.8	2.3 2.8	11.1 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	4.3 3.5	9.0 9.8	12.0 12.3	4.3 3.5	14.2 15.1	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	3.0 3.0	7.6 7.4	10.5 9.6	3.0 3.0	12.4 11.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	2.9 3.0	6.9 6.8	9.4 8.6	2.9 3.0	11.0 10.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	4.8 4.5	11.0 10.6	14.3 13.6	4.8 4.5	16.8 16.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	3.3 3.9	8.4 8.7	11.8 11.2	3.3 3.9	14.1 13.1	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	3.9 4.0	9.6 9.0	12.8 11.4	3.9 4.0	15.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	5.0 4.9	13.1 11.9	18.3 16.3	5.0 4.9	21.8 19.4	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	5.6 6.2	14.0 15.3	19.2 20.2	5.6 6.2	22.7 24.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	3.4 3.5	10.2 9.0	13.6 11.6	3.4 3.5	15.8 13.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	5.4 5.2	13.8 12.2	17.9 15.9	5.4 5.2	21.3 19.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	5.9 6.6	14.2 15.8	18.8 19.7	5.9 6.6	23.0 23.7	ns
t_S	Setup time, High or Low D_n to $\overline{PL}$		6	3.5			3.5		ns
t_h	Hold time, High or Low D_n to $\overline{PL}$		6	0.5			0.5		ns
t_S	Setup time, High or Low $\overline{CE}$ to CP		6	11.5			11.5		ns
t_h	Hold time, High or Low $\overline{CE}$ to CP		6	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{U}$/D to CP		6	12.0			12.0		ns
t_h	Hold time, High or Low $\overline{U}$/D to CP		6	0.0			0.0		ns
t_w	$\overline{PL}$ pulse width, Low		5	4.5			4.5		ns
t_w	CP pulse width, High or Low		1	8.3			8.3		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.5			2.5		ns

Asynchronous presettable synchronous decade up/down counter with single clock

74AC/ACT11190

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74AC11190					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	120	150		120		MHz
		CP to $\overline{RC}$, TC		75	100		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	1.8 2.1	4.9 5.4	7.3 7.7	1.8 2.1	8.1 8.8	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	3.0 3.3	6.0 6.7	8.6 9.1	3.0 3.3	9.7 10.4	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	2.1 2.6	5.1 5.2	7.6 7.2	2.1 2.6	8.6 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	2.5 2.8	4.9 5.1	7.0 6.9	2.5 2.8	7.8 7.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	4.1 4.0	7.3 7.2	10.1 10.1	4.1 4.0	11.2 11.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	2.9 3.4	5.6 6.2	8.7 8.3	2.9 3.4	9.7 9.4	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	3.0 3.1	6.3 6.3	8.1 8.6	3.0 3.1	10.1 9.6	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	4.3 4.1	8.3 8.0	12.4 11.4	4.3 4.1	14.0 13.3	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	4.8 5.2	9.0 9.8	13.2 13.9	4.0 5.2	14.8 15.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	3.1 2.9	6.4 6.2	9.5 8.8	3.1 2.9	10.4 9.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	4.9 4.4	8.8 8.2	12.3 11.5	4.9 4.4	13.8 12.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	5.3 5.8	9.1 10.1	12.8 13.6	5.3 5.8	14.4 15.3	ns
t_S	Setup time, High or Low D_n to $\overline{PL}$		6	2.5			2.5		ns
t_h	Hold time, High or Low D_n to $\overline{PL}$		6	0.5			0.5		ns
t_S	Setup time, High or Low $\overline{CE}$ to CP		6	7.5			7.5		ns
t_h	Hold time, High or Low $\overline{CE}$ to CP		6	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{U}$/D to CP		6	8.0			8.0		ns
t_h	Hold time, High or Low $\overline{U}$/D to CP		6	0.0			0.0		ns
t_w	$\overline{PL}$ pulse width, Low		5	3.5			3.5		ns
t_w	CP pulse width, High or Low		1	5.5			5.5		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.0			2.0		ns

Asynchronous presettable synchronous decade up/down counter with single clock

74AC/ACT11190

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74ACT11190					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	85	120		85		MHz
		CP to $\overline{RC}$, TC		65	90		65		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	3.7 4.2	7.0 7.6	9.1 9.7	3.7 4.2	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	4.8 5.4	8.3 9.1	10.7 11.5	4.8 5.4	11.8 12.7	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	4.2 3.6	7.7 6.9	10.1 9.7	4.2 3.6	11.0 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	3.9 3.0	6.6 6.1	8.9 8.4	3.9 3.0	9.7 9.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	4.9 4.5	8.7 8.6	11.8 11.6	4.9 4.5	12.9 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	3.5 4.1	7.0 7.5	10.2 10.0	3.5 4.1	11.5 11.3	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	4.6 4.0	7.9 7.3	10.2 10.3	4.6 4.0	11.4 11.6	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	5.1 4.9	9.7 9.6	13.7 13.2	5.1 4.9	15.2 14.6	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	5.7 6.4	10.6 11.3	14.7 15.0	5.7 6.4	16.2 16.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	4.1 4.1	7.6 7.6	10.7 10.5	4.1 4.1	11.8 11.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	5.4 5.0	9.9 9.5	13.7 13.0	5.4 5.0	15.2 14.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	5.9 6.6	10.4 11.5	14.6 15.1	5.9 6.6	16.4 16.8	ns
t_S	Setup time, High or Low D_n to $\overline{PL}$		6	2.5			2.5		ns
t_h	Hold time, High or Low D_n to $\overline{PL}$		6	1.5			1.5		ns
t_S	Setup time, High or Low $\overline{CE}$ to CP		6	7.0			7.0		ns
t_h	Hold time, High or Low $\overline{CE}$ to CP		6	1.5			1.5		ns
t_S	Setup time, High or Low $\overline{U}$/D to CP		6	7.5			7.5		ns
t_h	Hold time, High or Low $\overline{U}$/D to CP		6	0.0			0.0		ns
t_w	$\overline{PL}$ pulse width, Low		5	4.0			4.0		ns
t_w	CP pulse width, High or Low		1	7.7			7.7		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.0			2.0		ns

Asynchronous presettable synchronous decade up/down counter with single clock

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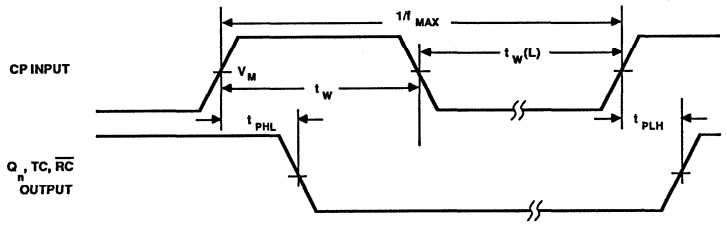
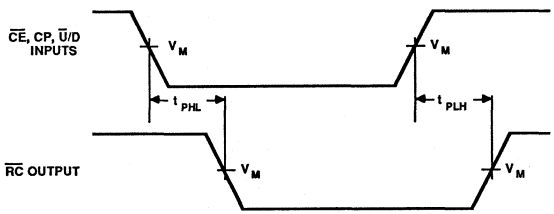
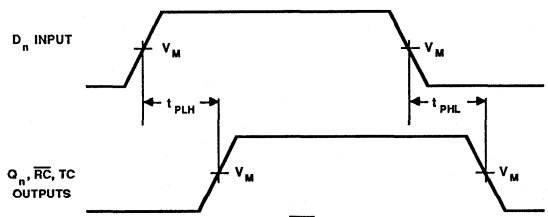
AC WAVEFORMS



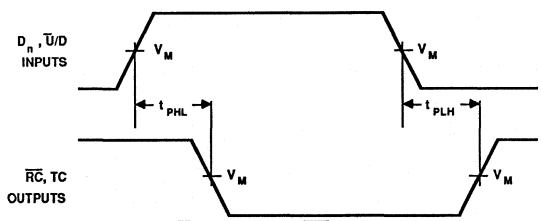
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Clock, Count Enable, or U/D to Ripple Clock Output Propagation Delay

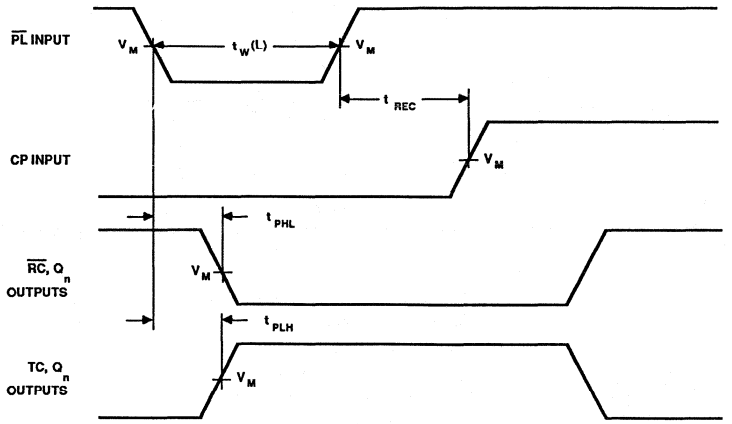


Waveform 3. Waveforms Showing the Input (D_n) to Output (Q_n, $\overline{RC}$, TC) Propagation Delays, Non-Inverting Path

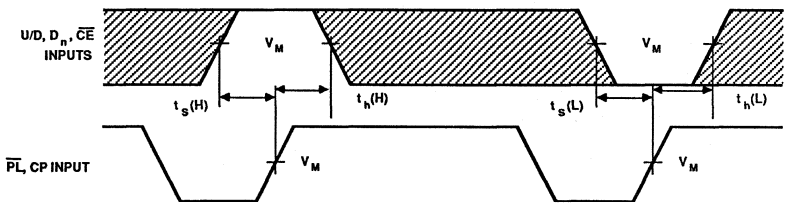


Waveform 4. Waveforms Showing the Input (D_n, $\overline{U}$/D) to Output ($\overline{RC}$, TC) Propagation Delays, Inverting Path

AC WAVEFORMS (Continued)



Waveform 5. Waveforms Showing the Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time



Waveform 6. Waveforms Showing Setup Time and Hold Time for D_n to $\overline{PL}$, $\overline{U}$/D to CP and $\overline{CE}$ to CP

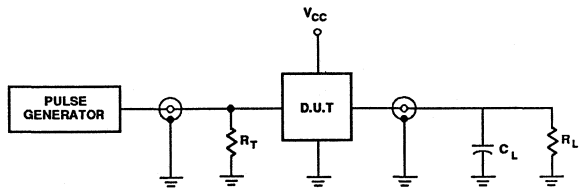
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

Asynchronous presettable synchronous decade up/down counter with single clock

74AC/ACT11190

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11191

Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

FEATURES

- Synchronous, reversible counting
- Positive edge-triggered clock
- 4-bit binary
- Asynchronous Parallel Load capability
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11191 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11191 is an asynchronously presettable up/down 4-bit binary counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = High)	C_L = 50pF	5.3	6.9	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	66	68	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency, CP → Q_n	C_L = 50pF	135	95	MHz

Note:

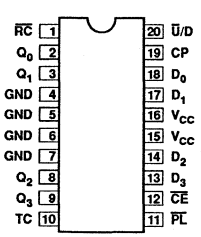
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

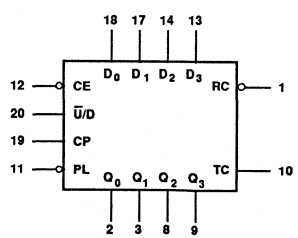
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11191N 74ACT11191N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11191D 74ACT11191D

PIN CONFIGURATION

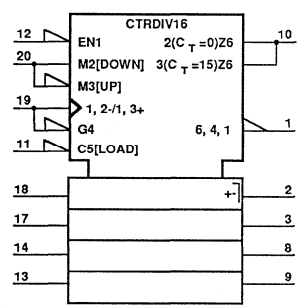
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

74AC/ACT11191

Asynchronous Parallel Load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a High level on the Count Enable ($\overline{CE}$) input.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally Low and goes High when: 1) the count reaches zero in the count-down mode or 2) reaches "15" in the Count-up mode. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the $\overline{RC}$ output. When TC is High and $\overline{CE}$ is Low, the $\overline{RC}$ follows the Clock Pulse. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays. The 74AC/ACT11191 simplifies the design of multistage counters, as indicated in Figures 1a and 1b.

In Figure 1a, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the Clock input source has limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any package goes High shortly after its CP input goes High, there is no such restriction on the High state duration of the clock.

In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.

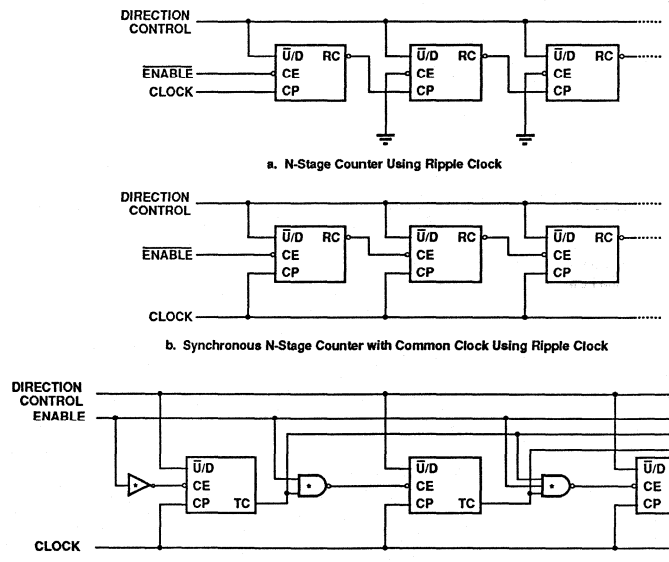


Figure 1

Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

74AC/ACT11191

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{U}$/D	Up/down count control input
12	$\overline{CE}$	Count enable input (active-Low)
18, 17, 14, 13	D_0 - D_3	Data inputs
19	CP	Clock pulse input (active rising edge)
11	$\overline{PL}$	Asynchronous load input (active-Low)
2, 3, 8, 9	Q_0 - Q_3	Counter outputs
1	$\overline{RC}$	Ripple clock output (active-Low)
10	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}$/D	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold (do nothing)	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE

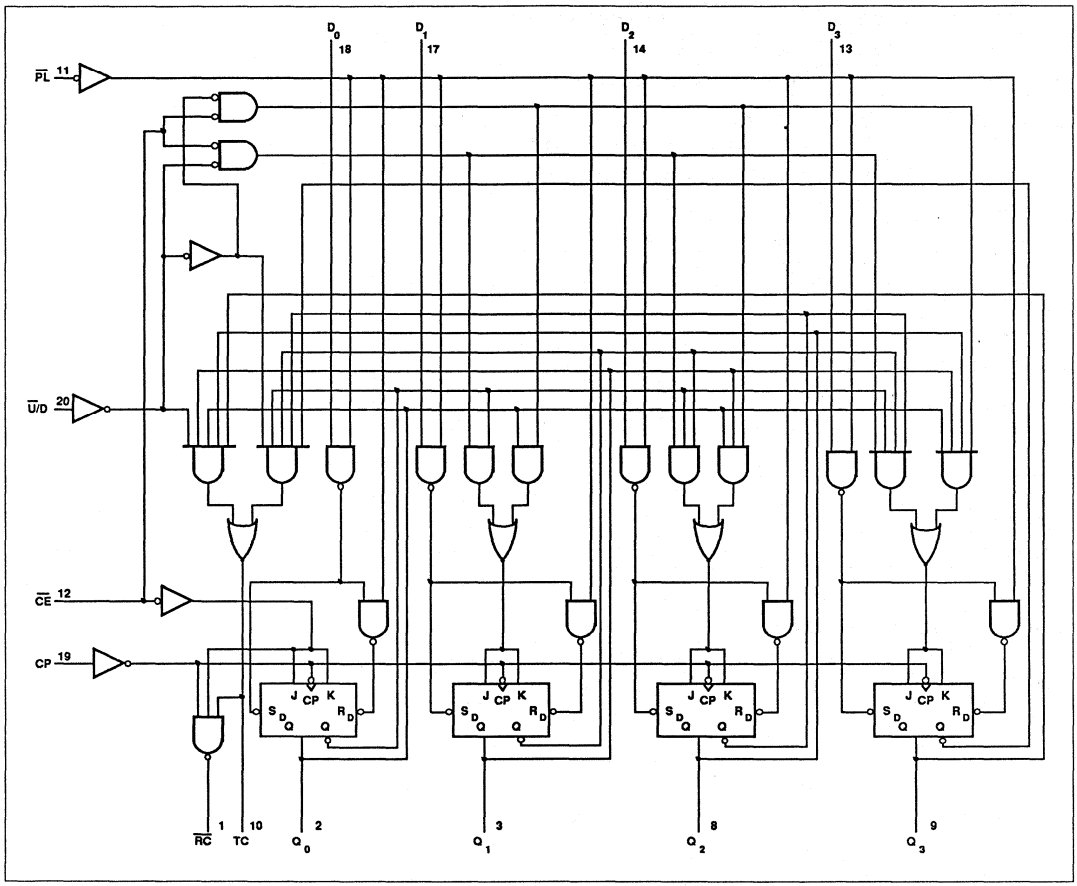
INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}$/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊓	H	H	H	H	H	⊓
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	H	⊓

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
↑ = Low-to-High clock transition
↓ = High-to-Low Trickle Clock transition
⊓ = Low pulse

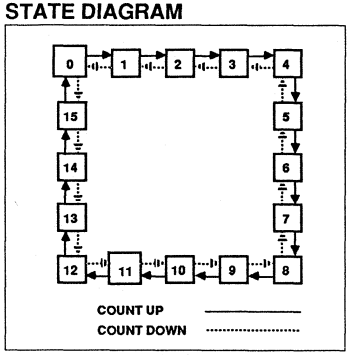
Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

74AC/ACT11191

LOGIC DIAGRAM



STATE DIAGRAM



Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

74AC/ACT11191

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11191			74ACT11191			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

74AC/ACT11191

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11191				74ACT11191				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER		WAVEFORM	74AC11191					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	50	80		50		MHz
		CP to $\overline{RC}$, TC		50	80		50		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	2.2 2.7	7.5 7.5	9.8 11.0	2.2 2.7	11.1 12.7	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	3.7 4.1	9.9 10.2	12.2 14.4	3.7 4.1	13.8 16.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	2.8 2.8	8.7 7.8	11.5 10.6	2.8 2.8	12.9 11.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	2.5 2.6	7.2 6.6	9.0 8.8	2.5 2.6	10.3 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	4.1 4.1	11.2 10.2	14.4 14.3	4.1 4.1	15.9 16.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	2.7 3.1	8.7 8.3	11.5 11.8	2.7 3.1	12.7 13.6	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	3.4 3.5	9.8 8.9	12.3 12.1	3.4 3.5	13.8 13.7	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	4.7 4.0	13.5 11.8	18.2 17.1	4.7 4.0	20.7 19.3	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	5.0 5.3	14.7 15.1	19.9 21.1	5.0 5.3	22.5 24.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	3.7 3.6	10.7 9.3	13.4 12.3	3.7 3.6	14.9 14.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	5.0 4.6	14.2 12.6	18.7 17.5	5.0 4.6	21.1 19.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	5.2 6.0	15.4 15.7	20.2 21.6	5.2 6.0	22.9 24.7	ns
t_S	Setup time, High or Low D_n to $\overline{PL}$		6	4.0			4.0		ns
t_h	Hold time, High or Low D_n to $\overline{PL}$		6	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{CE}$ to CP		6	12.5			12.5		ns
t_h	Hold time, High or Low $\overline{CE}$ to CP		6	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{U}$/D to CP		6	13.5			13.5		ns
t_h	Hold time, High or Low $\overline{U}$/D to CP		6	0.0			0.0		ns
t_w	$\overline{PL}$ pulse width, Low		5	4.8			4.8		ns
t_w	CP pulse width, High or Low		1	10.0			10.0		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.5			2.5		ns

Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

74AC/ACT11191

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74AC11191					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	100	135		100		MHz
		CP to $\overline{RC}$, TC		70	95		70		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	1.9 2.4	5.2 5.4	7.6 8.0	1.9 2.4	8.4 9.4	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	3.0 3.6	6.5 7.1	8.8 10.4	3.0 3.6	10.4 10.8	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	2.4 2.9	5.9 5.6	8.4 7.7	2.4 2.9	9.1 8.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	2.1 2.2	4.9 4.8	6.8 6.7	2.1 2.2	7.7 7.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	3.5 3.5	7.2 6.9	10.2 10.0	3.5 3.5	11.3 11.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	2.3 2.7	5.7 5.9	8.1 8.6	2.3 2.7	9.1 9.7	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	2.9 3.0	6.2 6.1	8.7 8.7	2.9 3.0	9.8 9.8	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	4.1 3.5	8.4 8.0	12.2 11.8	4.1 3.5	13.7 13.4	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	4.3 4.7	9.2 9.7	13.5 14.0	4.3 4.7	15.1 16.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	3.1 3.0	6.7 6.4	9.4 9.0	3.1 3.0	10.6 10.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	4.3 4.0	8.8 8.4	12.5 12.0	4.3 4.0	14.3 13.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	4.5 5.0	9.7 10.1	13.7 14.4	4.5 5.0	15.4 16.3	ns
t_s	Setup time, High or Low D_n to $\overline{PL}$		6	3.0			3.0		ns
t_h	Hold time, High or Low D_n to $\overline{PL}$		6	1.5			1.5		ns
t_s	Setup time, High or Low $\overline{CE}$ to CP		6	8.0			8.0		ns
t_h	Hold time, High or Low $\overline{CE}$ to CP		6	0.5			0.5		ns
t_s	Setup time, High or Low $\overline{U}$/D to CP		6	8.5			8.5		ns
t_h	Hold time, High or Low $\overline{U}$/D to CP		6	0.0			0.0		ns
t_w	$\overline{PL}$ pulse width, Low		5	4.0			4.0		ns
t_w	CP pulse width, High or Low		1	7.2			7.2		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.0			2.0		ns

Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

74AC/ACT11191

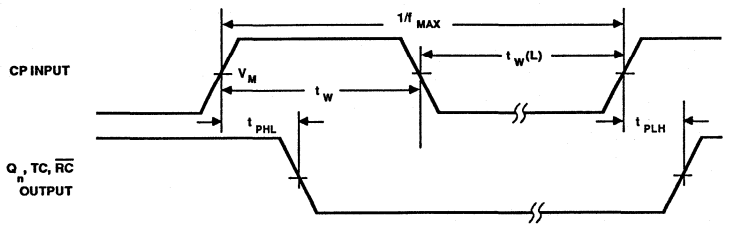
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74ACT11191					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	CP to Q_n	1	65	95		65		MHz
		CP to $\overline{RC}$, TC		65	95		65		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		1	3.6 4.2	6.7 7.1	9.2 9.4	3.6 4.2	10.4 10.8	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC		1	5.0 5.3	8.0 8.6	10.3 11.5	5.0 5.3	11.7 13.1	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$		2	4.4 3.5	7.4 6.7	9.5 9.5	4.4 3.5	11.0 10.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$		2	3.9 2.8	6.4 6.0	8.2 8.4	3.9 2.8	9.2 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$		2	4.4 4.2	8.4 8.8	11.7 11.3	4.4 4.2	13.1 13.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC		4	3.2 3.6	6.9 7.2	9.6 10.3	3.2 3.6	11.0 11.6	ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		3	4.5 3.7	7.6 7.1	10.1 10.3	4.5 3.7	11.6 11.7	ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC		3, 4	5.1 4.7	9.5 9.2	13.6 13.4	5.1 4.7	15.4 15.2	ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$		3, 4	5.5 5.9	10.3 10.9	14.8 15.5	5.5 5.9	17.2 18.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n		5	4.0 3.8	7.6 7.4	10.8 10.5	4.0 3.8	12.2 11.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC		5	5.2 4.7	9.7 9.5	13.9 13.6	5.2 4.7	15.8 15.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$		5	5.4 5.8	10.5 11.0	15.1 15.7	5.4 5.8	17.1 17.9	ns
t_S	Setup time, High or Low D_n to $\overline{PL}$		6	3.0			3.0		ns
t_h	Hold time, High or Low D_n to $\overline{PL}$		6	2.5			2.5		ns
t_S	Setup time, High or Low $\overline{CE}$ to CP		6	7.5			7.5		ns
t_h	Hold time, High or Low $\overline{CE}$ to CP		6	1.5			1.5		ns
t_S	Setup time, High or Low $\overline{U}$/D to CP		6	8.5			8.5		ns
t_h	Hold time, High or Low $\overline{U}$/D to CP		6	0.5			0.5		ns
t_w	$\overline{PL}$ pulse width, Low		5	4.0			4.0		ns
t_w	CP pulse width, High or Low		1	7.7			7.7		ns
t_{REC}	Recover time, $\overline{PL}$ to CP		5	2.0			2.0		ns

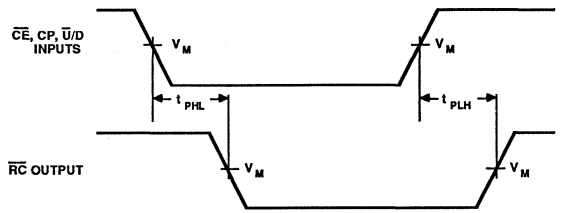
Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

74AC/ACT11191

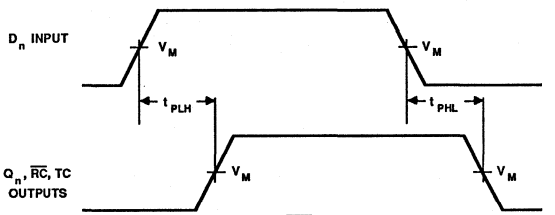
AC WAVEFORMS



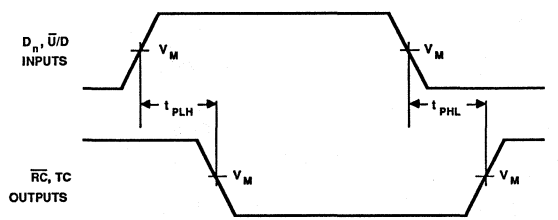
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Clock, Count Enable, or U/D to Ripple Clock Output Propagation Delay

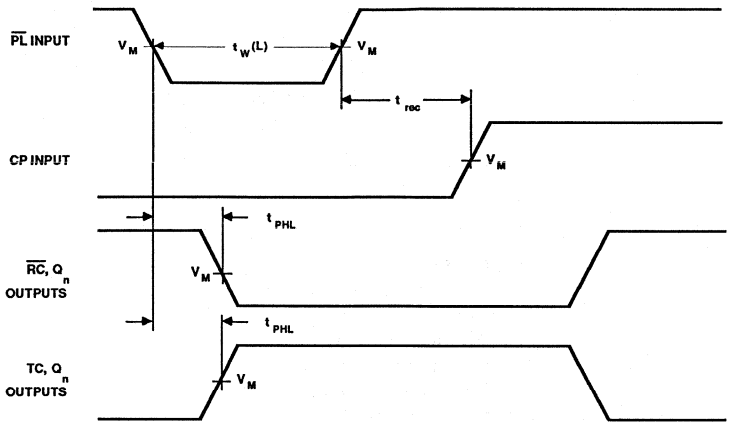


Waveform 3. Waveforms Showing the Input (D_n) to Output (Q_n, $\overline{RC}$, TC) Propagation Delays, Non-Inverting Path

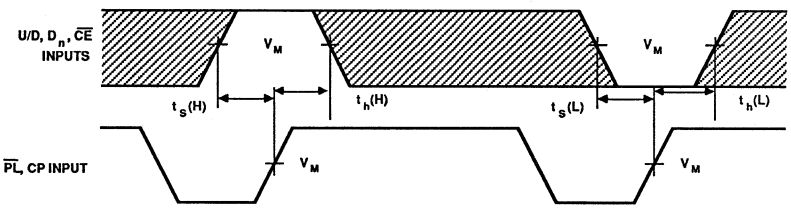


Waveform 4. Waveforms Showing the Input (D_n, $\overline{U}$/D) to Output ($\overline{RC}$, TC) Propagation Delays, Inverting Path

AC WAVEFORMS (continued)



Waveform 5. Waveforms Showing the Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time



Waveform 6. Waveforms Showing Setup Time and Hold Time for D_n to PL, U/D to CP and CE to CP

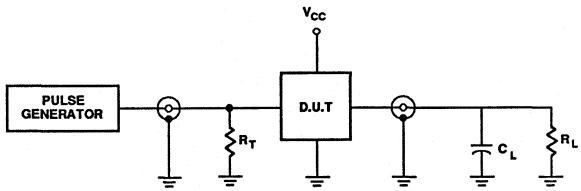
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

Asynchronous presettable synchronous 4-bit binary up/down counter with single clock

74AC/ACT11191

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11194

4-bit bidirectional universal shift register

FEATURES

- Shift left and shift right capability
- Synchronous Parallel and Serial data transfers
- Easily expanded for both Serial and Parallel operation
- Asynchronous reset
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11194 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11194 4-bit Bidirectional Universal Shift Register is fully synchronous, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n ($\overline{MR}$ = High)	C_L = 50pF	4.2	6.2	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	66	69	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	130	130	MHz

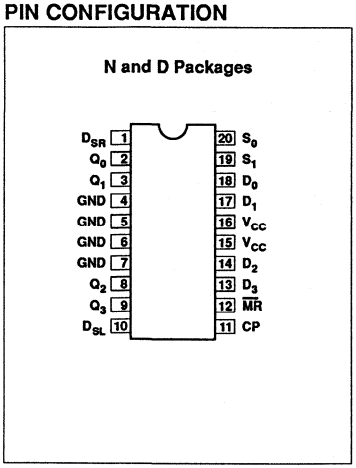
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

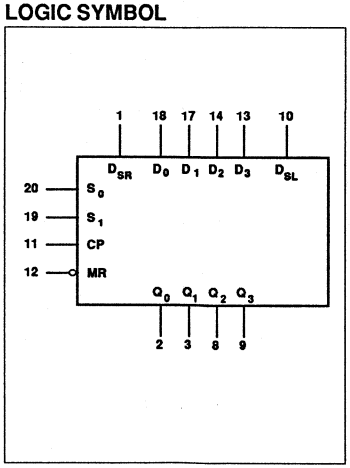
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11194N 74ACT11194N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11194D 74ACT11194D

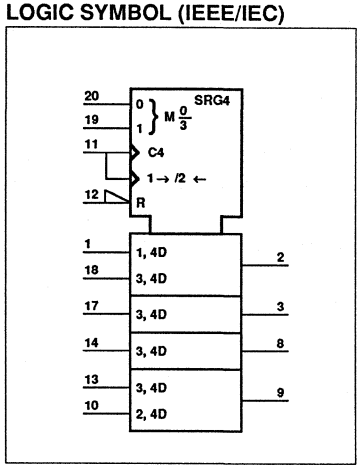
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



4-bit bidirectional universal shift register 74AC/ACT11194

The 74AC/ACT11194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Function Table, data can be entered and shifted from left to right (shift right, Q_0 Æ Q_1, etc.), or right to left (shift left, Q_3 Æ Q_2, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data input (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

The only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. Signals on the Select (S_0, S_1), Parallel Data (D_0 - D_3) and Serial Data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only the recommended setup and hold times, with respect to the clock rising edge are observed.

The four Parallel Data inputs (D_0 - D_3) are D-type inputs. Data appearing on D_0 - D_3 inputs when S_0 and S_1 are High is transferred to the Q_0 - Q_3 outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs Low.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
12	$\overline{MR}$	Asynchronous master reset (active Low)
11	CP	Clock input (Low-to-High, edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
1	D_{SR}	Serial data input (shift right)
10	D_{SL}	Serial data input (shift left)
20, 19	S_0, S_1	Mode control inputs
2, 3, 8, 9	Q_0 - Q_3	Parallel outputs outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

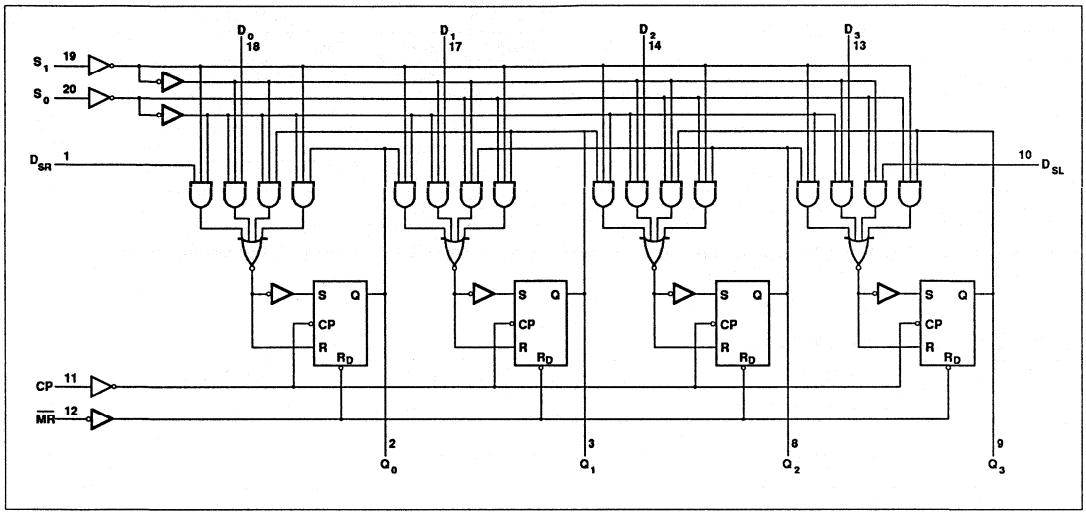
FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	↑	H	h	l	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	↑	H	l	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	↑	H	h	h	X	X	dn	d_0	d_1	d_2	d_3

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
d_n (q_n) = State of the referenced input (or output) one setup time prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

4-bit bidirectional universal shift register 74AC/ACT11194

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11194			74ACT11194			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11194				74ACT11194				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11194					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	90	120		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	1.0 1.0	5.8 6.6	8.4 8.9	1.0 1.0	9.5 10.2	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.7	7.1	9.5	1.7	10.7	ns
t_S	Setup time, High or Low D_n, D_{SR}, D_{SL} to CP	3	4.0			4.0		ns
t_H	Hold time, High or Low CP to D_n, D_{SR}, D_{SL}	3	0.5			0.5		ns
t_S	Setup time, High or Low S_n to CP	3	5.0			5.0		ns
t_H	Hold time, High or Low CP to S_n	3	1.5			1.5		ns
t_W	Clock pulse width (load) High or Low	1	5.5			5.5		ns
t_W	Clock pulse width (count) High or Low	1	5.5			5.5		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.0			1.0		ns

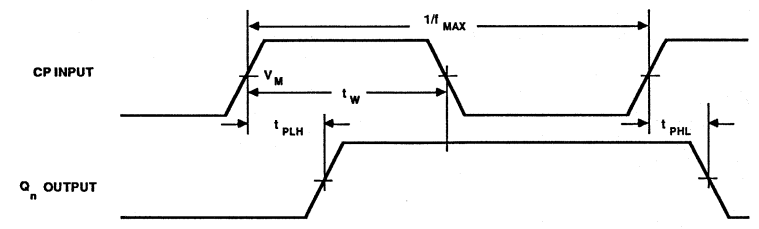
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11194					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	0.8 1.1	3.9 4.4	6.2 6.6	0.8 1.1	6.8 7.7	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	4.6	7.0	1.5	7.8	ns
t_S	Setup time, High or Low D_n, D_{SR}, D_{SL} to CP	3	2.5			2.5		ns
t_H	Hold time, High or Low CP to D_n, D_{SR}, D_{SL}	3	1.0			1.0		ns
t_S	Setup time, High or Low S_n to CP	3	4.0			4.0		ns
t_H	Hold time, High or Low CP to S_n	3	1.5			1.5		ns
t_W	Clock pulse width (load) High or Low	1	5.0			5.0		ns
t_W	Clock pulse width (count) High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

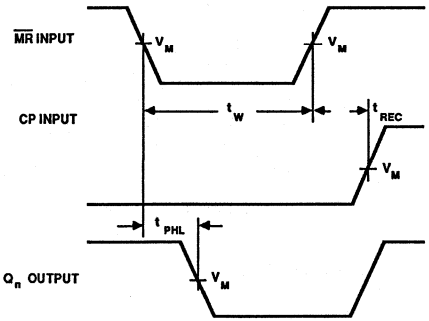
SYMBOL	PARAMETER	WAVEFORM	74ACT11194					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	2.2 2.6	5.8 6.6	6.9 7.7	2.2 2.6	7.7 8.8	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	2.9	7.1	9.1	2.9	10.3	ns
t_S	Setup time, High or Low D_n, D_{SR}, D_{SL} to CP	3	4.0			4.0		ns
t_H	Hold time, High or Low CP to D_n, D_{SR}, D_{SL}	3	1.0			1.0		ns
t_S	Setup time, High or Low S_n to CP	3	6.0			6.0		ns
t_H	Hold time, High or Low CP to S_n	3	1.5			1.5		ns
t_W	Clock pulse width (load) High or Low	1	5.0			5.0		ns
t_W	Clock pulse width (count) High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.0			1.0		ns

AC WAVEFORMS

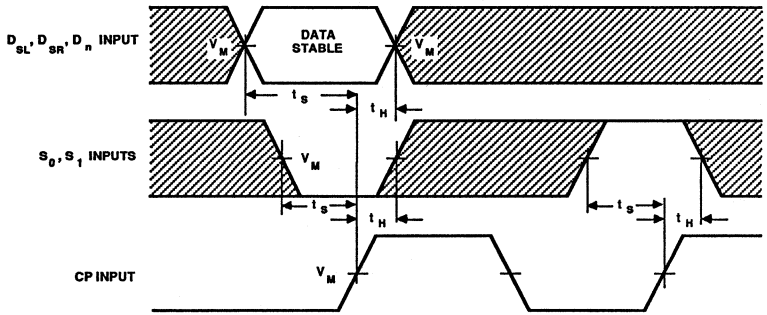


Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width

AC WAVEFORMS (Continued)



Waveform 2. Waveforms Showing the Master Reset ($\overline{MR}$) Pulse Width, the Master Reset to Output (Q_n) Propagation Delays, and the Master Reset to Clock (CP) Recovery Time

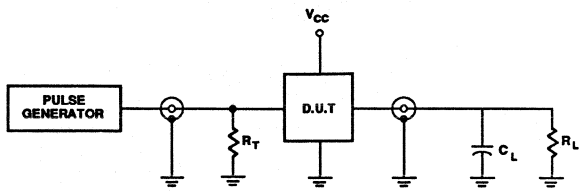


Waveform 3. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n, D_{SL}, D_{SR}) and for S_0 and S_1 Inputs

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	May 11, 1990
Status	Product Specification
ACL Products	

AC11239: Product Specification
ACT11239: Preliminary Specification
Dual 2-to-4 line decoder/demultiplexer, active-High

FEATURES

- Demultiplexing capability
- Two independent 1-of-4 decoders
- Non-inverting outputs
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11239 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11239 has two independent decoders, each accepting two binary weighted inputs (nA_0, nA_1) and providing four mutually exclusive active-High outputs (nY_0 - nY_3). Each decoder has an active-Low Enable ($n\overline{E}$). When $\overline{E}$ is High, every output is forced Low. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay nA_n to nY_n	C_L = 50pF	3.9	5.2	ns
C_{PD}	Power dissipation capacitance per decoder[1]	f = 1MHz; C_L = 50pF	48	50	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

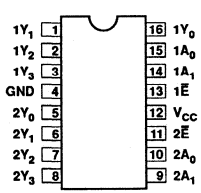
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

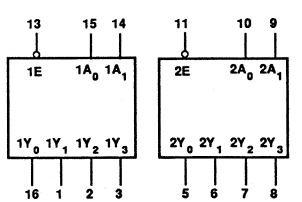
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11239N 74ACT11239N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11239D 74ACT11239D

PIN CONFIGURATION

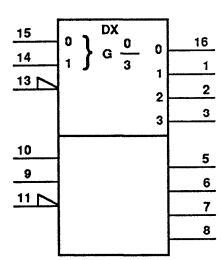
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Dual 2-to-4 line decoder/demultiplexer, active-High

74AC/ACT11239

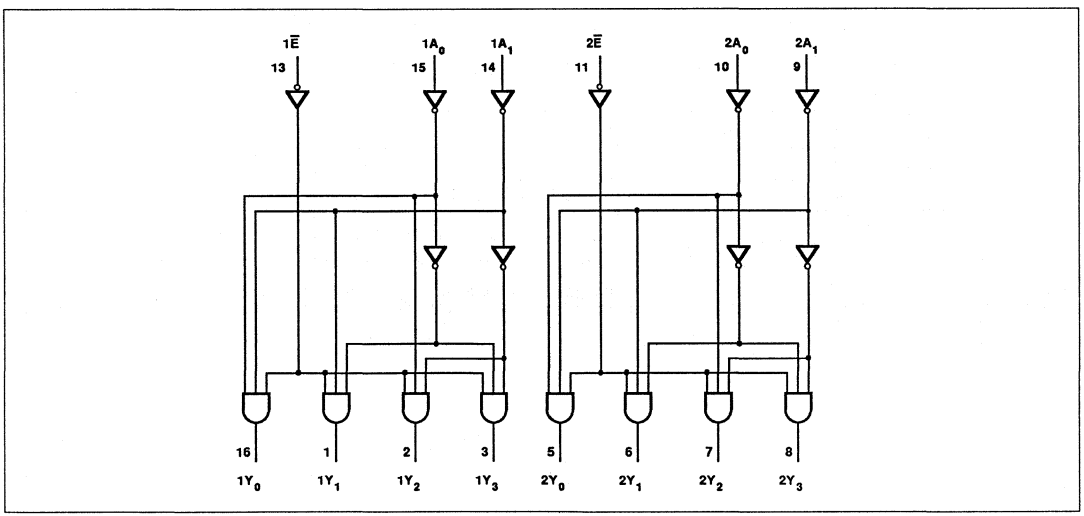
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15, 14	$1A_0$, $1A_1$	Address inputs, decoder 1
13	$1\overline{E}$	Enable input (active Low), decoder 1
16, 1, 2, 3	$1Y_0$ to $1Y_3$	Outputs, decoder 1
10, 9	$2A_0$, $2A_1$	Address inputs, decoder 2
11	$2\overline{E}$	Enable input (active Low), decoder 2
5, 6, 7, 8	$2Y_0$ to $2Y_3$	Outputs, decoder 2
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	Y_0	Y_1	Y_2	Y_3
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H

LOGIC DIAGRAM



Dual 2-to-4 line decoder/demultiplexer, active-High

74AC/ACT11239

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11239			74ACT11239			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Dual 2-to-4 line decoder/demultiplexer, active-High

74AC/ACT11239

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11239				74ACT11239				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Dual 2-to-4 line decoder/demultiplexer, active-High

74AC/ACT11239

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11239					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA_n to nY_n	1 and 2	1.5 1.5	6.2 5.6	8.5 8.0	1.5 1.5	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to nY_n	2	1.5 1.5	5.4 5.7	7.1 7.3	1.5 1.5	7.9 8.1	ns

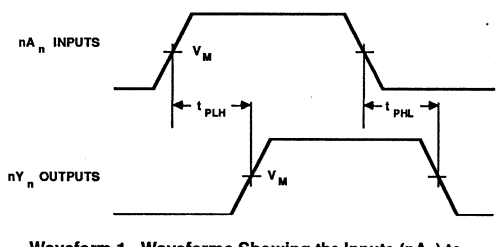
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11239					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA_n to nY_n	1 and 2	1.5 1.5	4.0 3.7	6.1 6.1	1.5 1.5	6.7 6.8	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to nY_n	2	1.5 1.5	3.5 3.9	5.3 5.6	1.5 1.5	5.8 6.2	ns

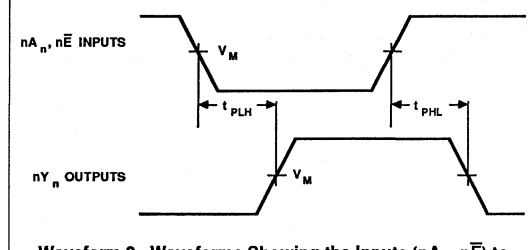
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11239					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA_n to nY_n	1 and 2	1.7 1.5	5.0 5.4	6.7 7.2	1.7 1.5	7.2 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $n\overline{E}$ to nY_n	2	1.5 2.6	3.8 5.3	5.8 7.1	1.5 2.6	6.2 7.8	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Inputs (nA_n) to Output (nY_n) Propagation Delays



Waveform 2. Waveforms Showing the Inputs (nA_n, $n\overline{E}$) to Output (nY_n) Propagation Delays

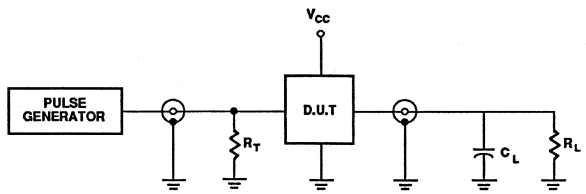
Dual 2-to-4 line decoder/demultiplexer, active-High

74AC/ACT11239

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11251

8-input multiplexer (3-State)

FEATURES

- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11251 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11251 provides an 8-to-1 multiplexer with three select lines and a common output enable. The state of the Select (S_n) inputs determines the particular input line from which the data comes. The Output Enable ($\overline{OE}$) input is active-Low. When $\overline{OE}$ is High, both the Y output and the $\overline{Y}$ output are in the High-impedance "OFF" state regardless of all other input conditions.

The device is the logic implementation of a single pole, 8 position switch where the position of the switch is determined by the logic levels supplied to the Select inputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay I_n to Y	C_L = 50pF		3.9	5.5	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	Enabled	55	60	pF
			Disabled	13	16	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		3.5	3.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		8.0	8.0	pF

Note:

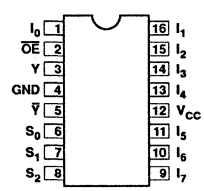
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

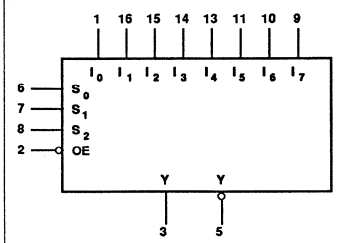
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11251N 74ACT11251N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11251D 74ACT11251D

PIN CONFIGURATION

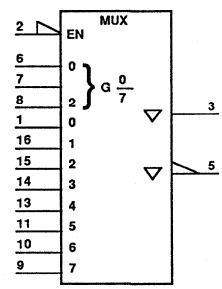
N and D Packages



LOGIC SYMBOL

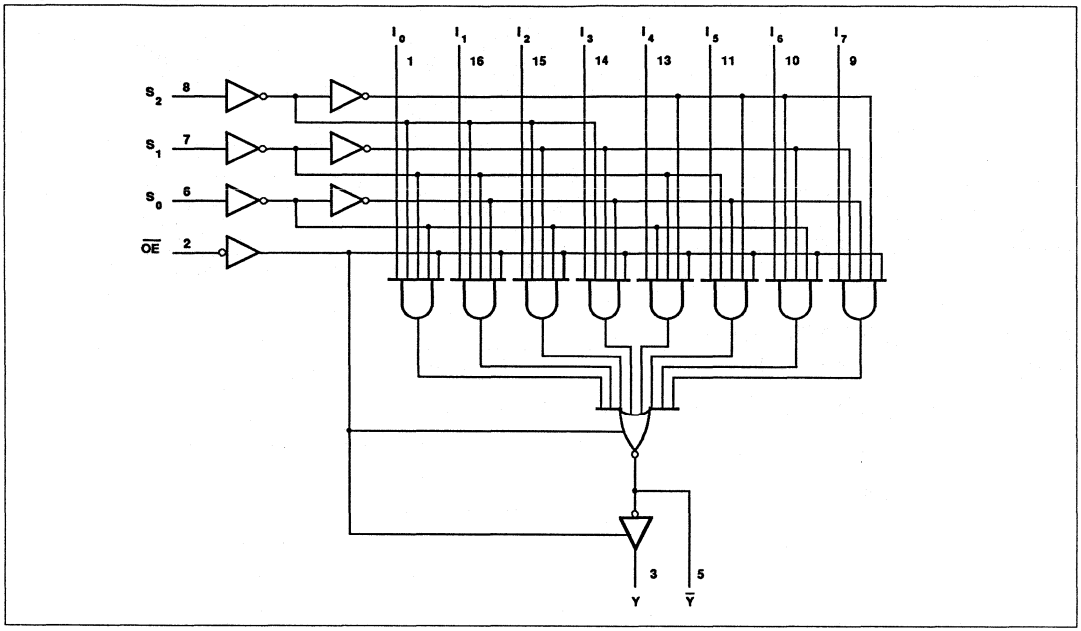


LOGIC SYMBOL (IEEE/IEC)



8-input multiplexer (3-State) 74AC/ACT11251

LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
6, 7, 8	S_n	Select inputs
2	$\overline{OE}$	Output enable input
1, 16, 15, 14 13, 11, 10, 9	$I_0 - I_7$	Data inputs
3, 5	Y, $\overline{Y}$	Data outputs
4	GND	Ground (0V)
12	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	
S_2	S_1	S_0	$\overline{OE}$	Y	$\overline{Y}$
X	X	X	H	Z	Z
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11151			74ACT11151			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11251				74ACT11251				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off–state current	$V_I = V_{IL}$ or V_{IH}, $V_O = V_{CC}$ or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

8-input multiplexer (3-State) 74AC/ACT11251

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11251					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	1	2.2 2.0	6.3 6.1	8.2 8.0	2.2 2.0	9.0 8.8	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	1	1.7 2.1	5.7 6.3	7.5 8.2	1.7 2.1	8.2 9.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	1	2.6 2.8	8.1 8.3	10.8 10.8	2.6 2.8	12.1 11.9	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	1	2.6 2.5	7.9 8.0	10.2 10.8	2.6 2.5	11.3 12.1	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to Y	2	1.3 1.6	4.1 4.9	5.7 6.6	1.3 1.6	6.1 7.2	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.2 1.5	4.0 4.8	5.5 6.5	1.2 1.5	5.9 7.1	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to Y	2	2.9 2.7	4.5 4.7	5.9 6.3	2.9 2.7	6.1 6.6	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	2.9 2.8	4.5 4.7	5.9 6.3	2.9 2.8	6.2 6.6	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

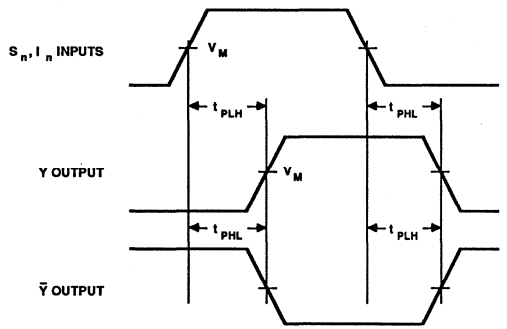
SYMBOL	PARAMETER	WAVEFORM	74AC11251					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	1	1.8 1.7	4.0 3.8	5.9 5.7	1.8 1.7	6.5 6.3	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	1	1.4 1.7	3.5 4.1	5.4 5.9	1.4 1.7	5.8 6.6	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	1	2.2 2.4	5.3 5.0	7.5 7.5	2.2 2.4	8.3 8.4	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	1	2.1 2.2	4.7 5.4	7.1 7.5	2.1 2.2	7.9 8.5	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to Y	2	1.0 1.3	2.7 3.1	4.4 4.8	1.0 1.3	4.7 5.2	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.0 1.2	2.6 3.0	4.3 4.7	1.0 1.2	4.6 5.1	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to Y	2	2.8 2.6	4.2 4.2	5.6 5.7	2.8 2.6	5.9 6.0	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	2.8 2.7	4.3 4.2	5.7 5.7	2.8 2.7	6.0 5.9	ns

8-input multiplexer (3-State) 74AC/ACT11251

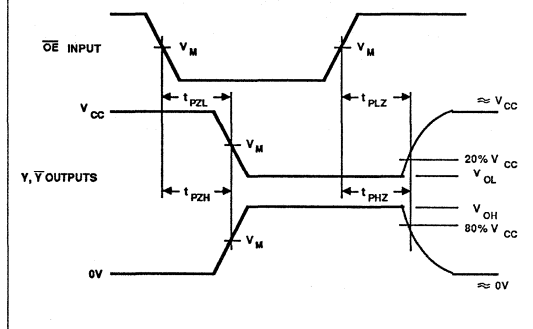
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11251					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y	1	3.0 2.0	5.7 5.2	7.8 7.9	3.0 2.0	8.7 8.6	ns
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}$	1	1.7 2.7	4.7 5.1	7.1 7.2	1.7 2.7	7.8 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y	1	3.2 2.7	6.8 6.7	10.2 9.5	3.2 2.7	11.4 10.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{Y}$	1	2.5 2.8	6.3 6.3	8.8 9.7	2.5 2.8	9.8 10.8	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to Y	2	1.3 1.3	3.7 4.0	6.2 6.0	1.3 1.3	6.8 6.8	ns
t_{PZH} t_{PZL}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	1.0 1.3	4.4 4.1	6.4 5.8	1.0 1.3	7.0 6.4	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to Y	2	4.1 3.1	5.7 4.0	7.6 6.6	4.1 3.1	8.1 6.9	ns
t_{PHZ} t_{PLZ}	Propagation delay $\overline{OE}$ to $\overline{Y}$	2	4.1 3.2	5.7 4.1	7.7 6.6	4.1 3.2	8.2 6.9	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Data Inputs (I_n) and Select Input (S_n) to Output (Y, $\overline{Y}$) Propagation Delays



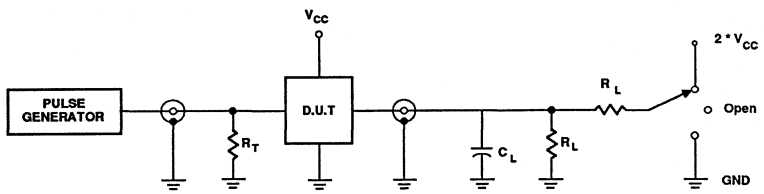
Waveform 2. Waveforms Showing the Output Enable Input ($\overline{OE}$) to Output (Y, $\overline{Y}$) Propagation Delays

8-input multiplexer (3-State) 74AC/ACT11251

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11286

9-bit odd/even parity generator/ checker with bus drive I/O port

FEATURES

- Generates either odd or even parity for nine data lines
- Word length easily expanded by cascading
- Direct bus connection for parity generation or for checking by using the parity I/O port
- Glitch-free bus during power up/down
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11286 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11286 9-bit parity generator or checker is commonly used to detect errors in high-speed data transmission or data retrieval systems. It fea-

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay I_n to PARITY ERROR	C_L = 50pF		5.9	7.3	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	Enabled	53	56	pF
			Disabled	46	50	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		3.5	3.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		8.5	8.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

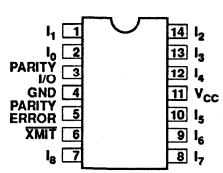
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

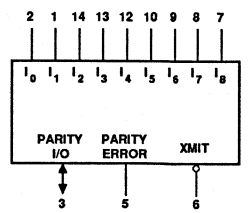
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11286N 74ACT11286N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11286D 74ACT11286D

PIN CONFIGURATION

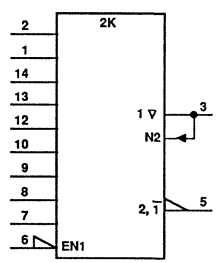
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



9-bit odd/even parity generator/checker with bus drive I/O port

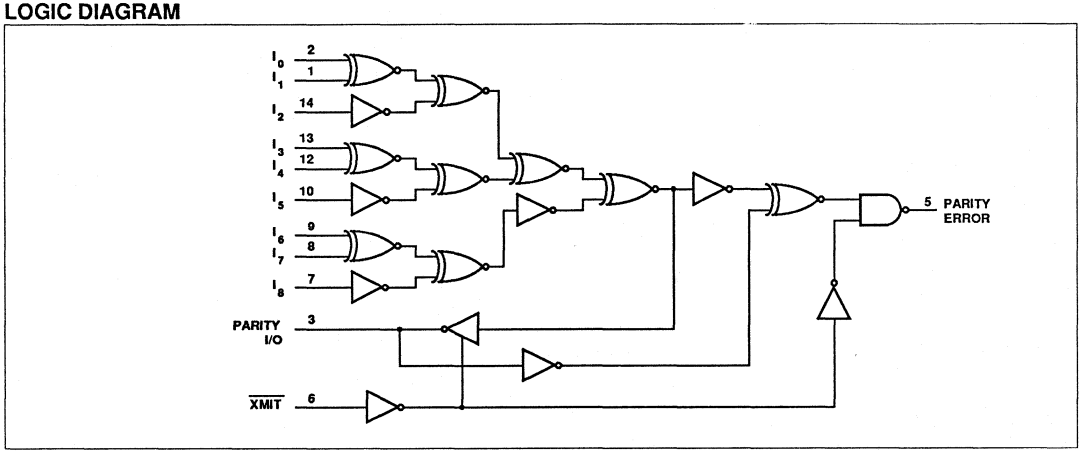
74AC/ACT11286

tures a local output for parity checking and a bus-driving parity I/O port for parity generation/checking.

The $\overline{XMIT}$ control input is implemented specifically for cascading for expanding word length. When $\overline{XMIT}$ is held Low the parity tree is disabled and the Parity Error output remains at a High logic level regardless of the other inputs (I_0 - I_8). When $\overline{XMIT}$ is High the parity tree is enabled. Parity Error indicates a parity error when either an even number of inputs are High and Parity I/O is forced to Low, or when an odd number of inputs are High and Parity I/O is forced High.

The I/O control circuitry is designed so that the I/O port will remain in the high-impedance state during power-up or power-down to prevent bus glitches.

LOGIC DIAGRAM



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 1, 14, 13, 12, 10, 9, 8, 7	I_0 - I_8	Data inputs
3	PARITY I/O	Parity I/O
6	$\overline{XMIT}$	Transmit input (active Low)
5	PARITY ERROR	Parity error output
4	GND	Ground (0V)
11	V_{CC}	Positive supply voltage

FUNCTION TABLE

Number of High Data Inputs (I_0 - I_8)	$\overline{XMIT}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

l = Low voltage level input
h = High voltage level input
H = High voltage level output
L = Low voltage level output

9-bit odd/even parity generator/checker with bus drive I/O port

74AC/ACT11286

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11286			74ACT11286			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9-bit odd/even parity generator/checker with bus drive I/O port

74AC/ACT11286

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11286				74ACT11286				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off–state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

9-bit odd/even parity generator/checker with bus drive I/O port

74AC/ACT11286

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11286					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY I/O	1	2.6 3.8	10.0 11.6	11.7 14.5	2.6 3.8	13.1 16.1	ns
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY ERROR	1	3.0 4.0	8.5 10.9	13.1 16.0	3.0 4.0	14.7 17.8	ns
t_{PLH} t_{PHL}	Propagation delay PARITY I/O to PARITY ERROR	1	2.2 3.4	5.9 7.9	7.6 10.2	2.2 3.4	8.4 11.1	ns
t_{PZH} t_{PHZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.8 3.2	4.9 5.4	6.4 6.6	1.8 3.2	7.0 7.0	ns
t_{PZL} t_{PLZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	3.5 3.2	9.7 5.4	12.8 6.7	3.5 3.2	13.6 7.2	ns

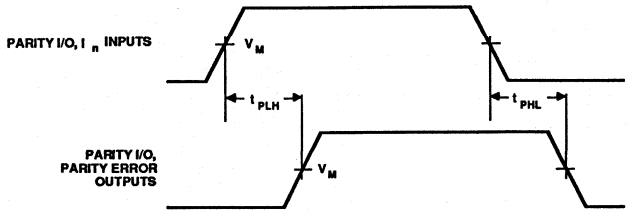
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11286					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY I/O	1	2.0 3.1	5.5 6.9	8.0 9.1	2.0 3.1	9.0 10.7	ns
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY ERROR	1	2.5 3.3	5.2 6.5	8.9 10.7	2.5 3.3	10.0 12.0	ns
t_{PLH} t_{PHL}	Propagation delay PARITY I/O to PARITY ERROR	1	1.9 2.9	3.9 5.0	5.6 7.2	1.9 2.9	6.2 7.9	ns
t_{PZH} t_{PHZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.4 3.1	3.3 4.8	4.9 6.1	1.4 3.1	5.3 6.5	ns
t_{PZL} t_{PLZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	3.0 3.0	5.4 4.6	8.3 6.0	3.0 3.0	8.9 6.3	ns

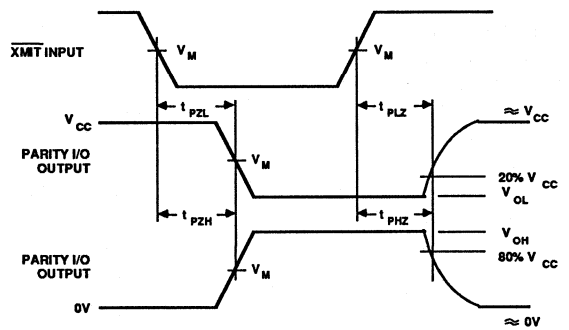
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11286					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY I/O	1	2.7 3.6	6.1 7.3	8.0 10.8	2.7 3.6	10.4 12.0	ns
t_{PLH} t_{PHL}	Propagation delay I_n to PARITY ERROR	1	3.0 3.9	6.9 7.7	9.7 11.4	3.0 3.9	11.3 12.9	ns
t_{PLH} t_{PHL}	Propagation delay PARITY I/O to PARITY ERROR	1	2.2 3.1	4.6 5.6	6.8 8.3	2.2 3.1	7.7 9.1	ns
t_{PZH} t_{PHZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	1.8 4.7	4.2 6.5	6.3 7.9	1.8 4.7	7.3 8.5	ns
t_{PZL} t_{PLZ}	Propagation delay $\overline{XMIT}$ to PARITY I/O	2	3.0 4.1	6.3 6.0	9.4 7.3	3.0 4.1	11.4 7.8	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Inputs (I_n, PARITY I/O) to Outputs (PARITY ERROR, PARITY I/O) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

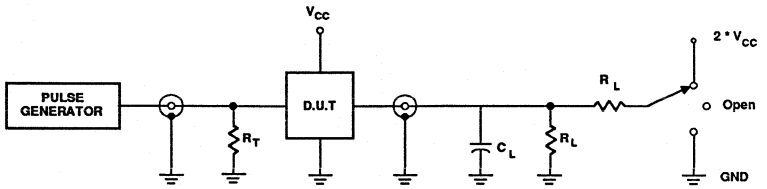
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

9-bit odd/even parity generator/checker with bus drive I/O port

74AC/ACT11286

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2*V_{CC}$
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

Date of Issue	July 30, 1990
Status	Preliminary Specification
ACL Products	

74AC11377

Octal D-type flip-flop with enable

FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered clock enable
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11377 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11377 provides eight positive edge-triggered D-type flip-flops with individual Data inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) is Low.

The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF	7.2		ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	72		pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	100		MHz

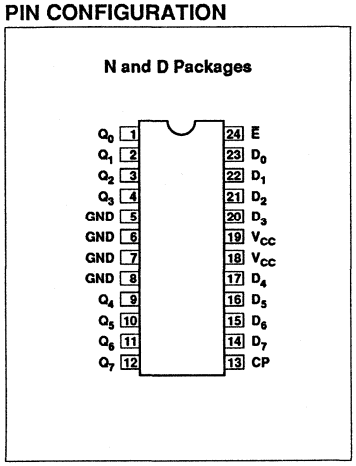
Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

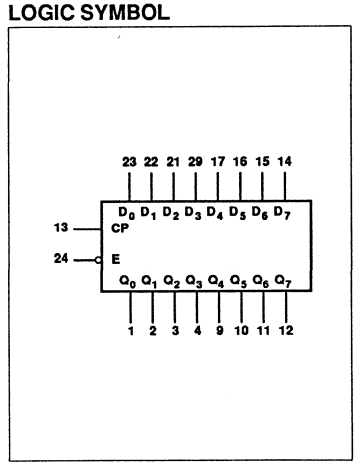
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11377N 74ACT11377N
24-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11377D 74ACT11377D

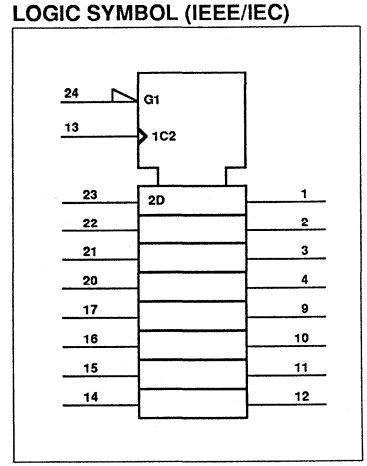
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal D-type flip-flop with enable 74AC/ACT11377

PIN DESCRIPTION

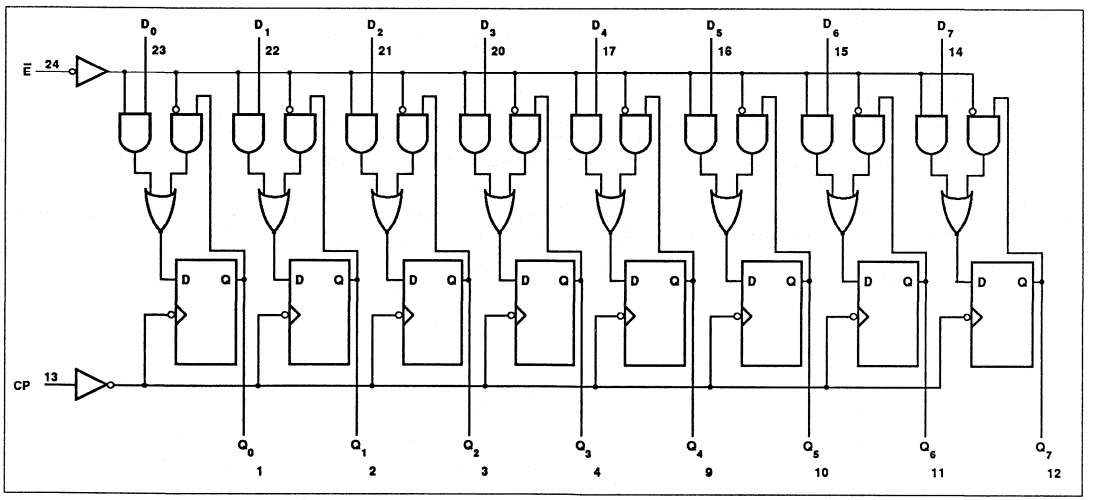
PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	$\overline{E}$	Enable input (active-Low)
13	CP	Clock pulse input
23, 22, 21, 20, 17, 16, 15, 14	D_0 - D_7	Data inputs
1, 2, 3, 4, 9, 10, 11, 12	Q_0 - Q_7	Data outputs
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{E}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑ X	h H	X X	no change no change

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ =Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11377			74ACT11377			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11377				74ACT11377				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Octal D-type flip-flop with enable 74AC/ACT11377

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11377					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	60			60		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	4.0 4.9	9.8 11.4	15.7 18.0	4.0 4.9	17.9 19.9	ns
t_S	Setup time, High or Low D_n to CP	2	6.0			6.0		ns
t_H	Hold time, High or Low D_n to CP	2	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{E}$ to CP	2	9.0			9.0		ns
t_H	Hold time, High or Low $\overline{E}$ to CP	2	0.0			0.0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns

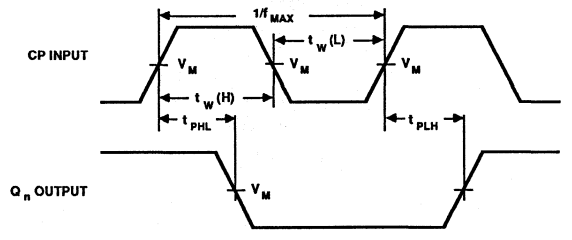
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11377					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100			100		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	3.3 4.1	6.6 7.8	9.9 11.5	3.3 4.1	11.3 12.9	ns
t_S	Setup time, High or Low D_n to CP	2	4.0			4.0		ns
t_H	Hold time, High or Low D_n to CP	2	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{E}$ to CP	2	6.0			6.0		ns
t_H	Hold time, High or Low $\overline{E}$ to CP	2	0.0			0.0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns

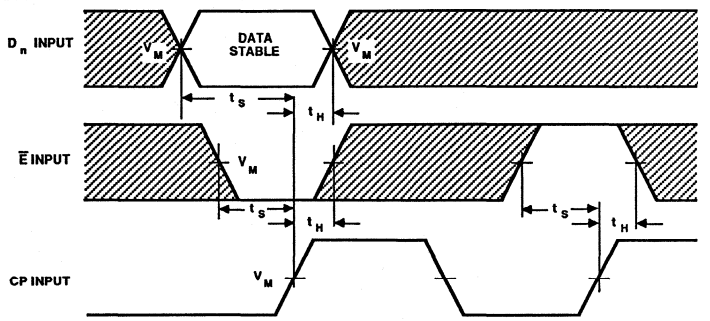
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11377					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	4.5 4.8	9.1 9.6	12.2 12.7	4.5 4.8	13.8 14.2	ns
t_S	Setup time, High or Low D_n to CP	2	4.0			4.0		ns
t_H	Hold time, High or Low D_n to CP	2	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{E}$ to CP	2	5.0			5.0		ns
t_H	Hold time, High or Low $\overline{E}$ to CP	2	0.0			0.0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns

WAVEFORMS



Waveform 1. Waveforms Showing the Propagation Delay, Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n) and Parallel Enable Input ($\overline{E}$)

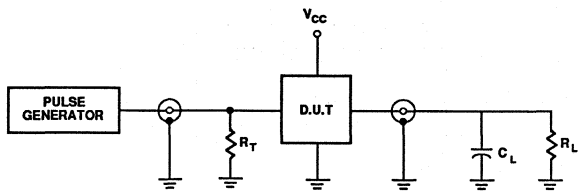
Octal D-type flip-flop with enable

74AC/ACT11377

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11378

Hex D-type flip-flop with enable, positive-edge trigger

FEATURES

- Output capability: ±24 mA
- Positive edge-triggered clock
- Common asynchronous Enable ($\overline{E}$) input
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11378 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11378 provides six edge-triggered D-type flip-flops with individual Data inputs (D_0 - D_5) and Q outputs (Q_0 - Q_5). The flip-flops load the data on the rising edge of the common clock (CP) providing that the common Enable ($\overline{E}$) is held Low. When the Enable is High, the flip-flops hold their previous state.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF	5.5	6.4	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	30	31	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50 pF	140	130	MHz

Note:

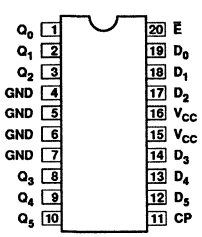
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

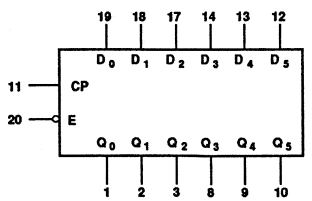
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11378N 74ACT11378N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11378D 74ACT11378D

PIN CONFIGURATION

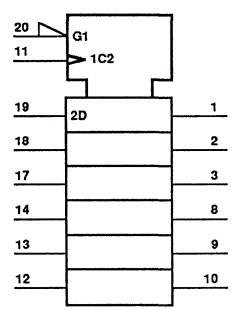
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Hex D-type flip-flop with enable, positive-edge trigger

74AC/ACT11378

PIN DESCRIPTION

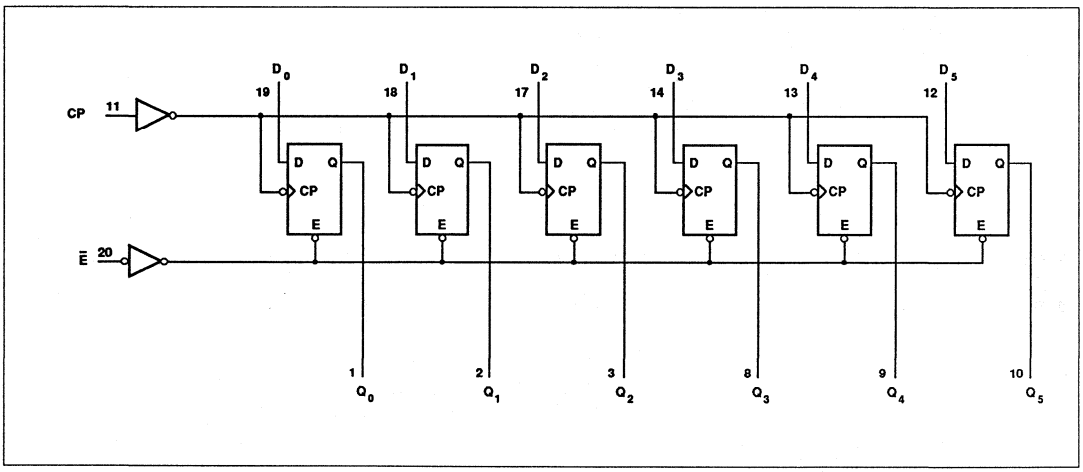
PIN NUMBER	SYMBOL	NAME AND FUNCTION
19, 18, 17, 14, 13, 12	D_0 - D_5	Data inputs
1, 2, 3, 8, 9, 10	Q_0 - Q_5	Data outputs
20	$\overline{E}$	Data enable input (active Low)
11	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{E}$	CP	D_n	Q_n
Disabled input (hold)	H	↑	X	NC
Load "1" (set)	L	↑	h	H
Load "0" (reset)	L	↑	l	L

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
NC = No Change
↑ = Low-to-High clock transition

LOGIC DIAGRAM



Hex D-type flip-flop with enable, positive-edge trigger

74AC/ACT11378

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11378			74ACT11378			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±150	mA
	DC ground current		±150	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Hex D-type flip-flop with enable, positive-edge trigger

74AC/ACT11378

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11378				74ACT11378				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Hex D-type flip-flop with enable, positive-edge trigger

74AC/ACT11378

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11378					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	90	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	3.0 3.6	7.6 9.8	9.5 12.8	3.0 3.6	10.9 14.0	ns
t_S	Setup time, High or Low D_n to CP	1	8.0			8.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{E}$ to CP	1	6.5			6.5		ns
t_H	Hold time, High or Low $\overline{E}$ to D_n	1	0.0			0.0		ns
t_W	Clock pulse width High or Low	1	5.5			5.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11378					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	140		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	2.4 3.0	5.0 6.0	7.0 8.8	2.4 3.0	7.7 9.7	ns
t_S	Setup time, High or Low D_n to CP	1	5.0			5.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{E}$ to CP	1	4.5			4.5		ns
t_H	Hold time, High or Low $\overline{E}$ to D_n	1	0.0			0.0		ns
t_W	Clock pulse width High or Low	1	4.5			4.5		ns

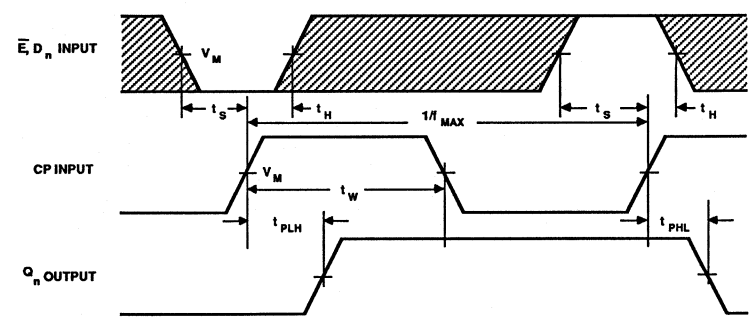
Hex D-type flip-flop with enable, positive-edge trigger

74AC/ACT11378

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11378					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	2.4 4.5	4.9 7.8	7.4 10.0	2.4 4.5	8.3 11.0	ns
t_S	Setup time, High or Low D_n to CP	1	5.0			5.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.5			0.5		ns
t_S	Setup time, High or Low $\overline{E}$ to CP	1	4.5			4.5		ns
t_H	Hold time, High or Low $\overline{E}$ to D_n	1	1.0			1.0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing Clock to Output Delays, Data Setup, and Clock Pulse Width

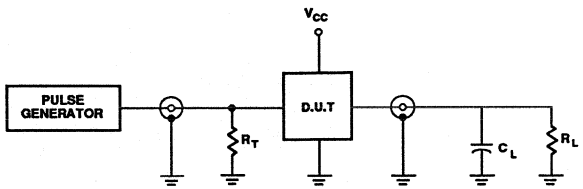
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

Hex D-type flip-flop with enable, positive-edge trigger

74AC/ACT11378

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11379

Quad D-type flip-flop with data enable

FEATURES

- Output capability: ±24 mA
- Edge-triggered D-type inputs
- Positive edge-triggered clock
- Common asynchronous Enable ($\overline{E}$) input
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11379 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11379 provides four edge-triggered D-type flip-flops with individual Data inputs (D_0 - D_3) and Q and $\overline{Q}$ outputs. The flip-flops load the data on the rising edge of the common clock (CP) providing that the common Enable ($\overline{E}$) is held Low. When the Enable is High, the flip-flops hold their previous state.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	C_L = 50pF	5.3	6.1	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	38	38	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	130	125	MHz

Note:

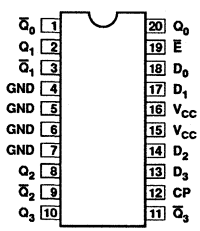
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

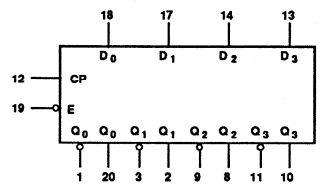
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11379N 74ACT11379N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11379D 74ACT11379D

PIN CONFIGURATION

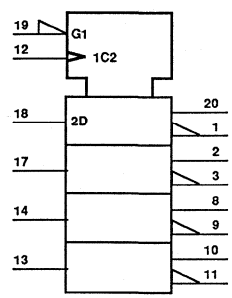
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Quad D-type flip-flop with data enable 74AC/ACT11379

PIN DESCRIPTION

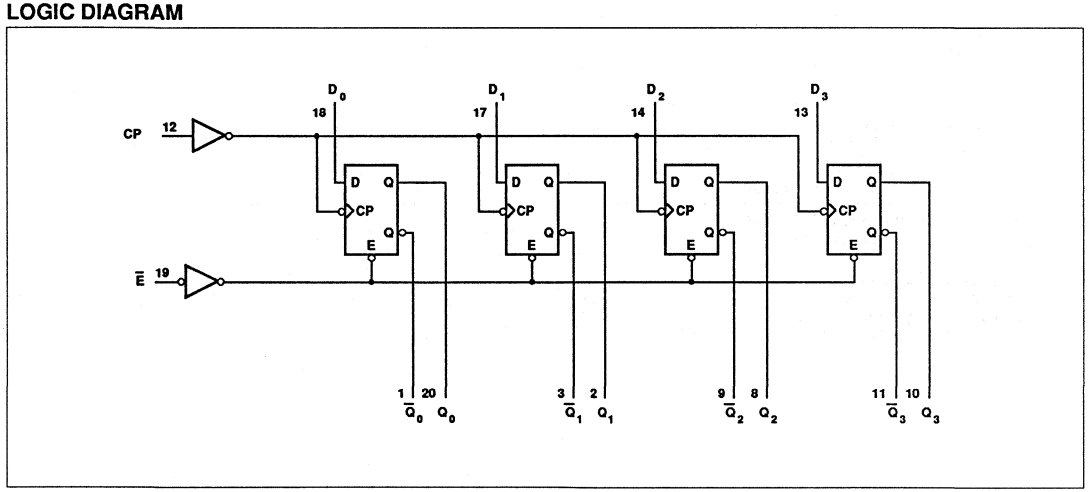
PIN NUMBER	SYMBOL	NAME AND FUNCTION
18, 17, 14, 13	D_0 - D_3	Data inputs
20, 2, 8, 10	Q_0 - Q_3	Data outputs
1, 3, 9, 11	$\overline{Q}_0$ - $\overline{Q}_3$	Data outputs (complements of Q_n outputs)
19	$\overline{E}$	Data enable input (active Low)
12	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
Disabled input (hold)	H	↑	X	NC	NC
Load "1" (set)	L	↑	h	H	L
Load "0" (reset)	L	↑	l	L	H

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
NC = No Change
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11379			74ACT11379			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11379				74ACT11379				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11379					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	90	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n , $\overline{Q}_n$	1	1.8 3.0	6.7 9.5	8.4 13.0	1.8 3.0	9.9 14.0	ns
t_S	Setup time, High or Low D_n to CP	1	7.5			7.5		ns
t_H	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{E}$ to CP	1	4.5			4.5		ns
t_H	Hold time, High or Low CP to $\overline{E}$	1	0.0			0.0		ns
t_W	Clock pulse width High or Low	1	5.5			5.5		ns

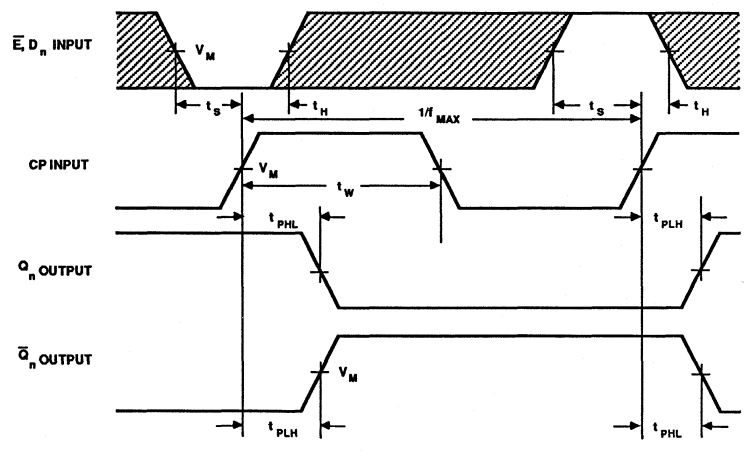
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11379					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	130		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n , $\overline{Q}_n$	1	1.5 2.6	4.3 6.2	6.0 9.1	1.5 2.6	6.7 10.3	ns
t_S	Setup time, High or Low D_n to CP	1	5.0			5.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{E}$ to CP	1	3.0			3.0		ns
t_H	Hold time, High or Low CP to $\overline{E}$	1	0.0			0.0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11379					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	2.2 3.1	5.0 7.2	6.6 9.8	2.2 3.1	7.4 11.2	ns
t_S	Setup time, High or Low D_n to CP	1	5.0			5.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_S	Setup time, High or Low $\overline{E}$ to CP	1	3.5			3.5		ns
t_H	Hold time, High or Low CP to $\overline{E}$	1	0.5			0.5		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns

AC WAVEFORMS

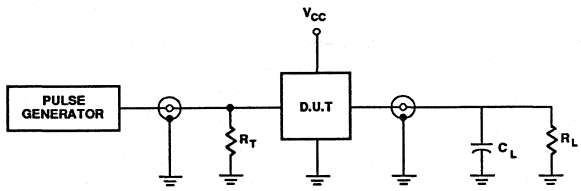


Waveform 1. Waveforms Showing Clock to Output Delays, Data and Enable Setup, and Clock Pulse Width

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f = 3ns$

Date of Issue	August 23, 1990
Status	Preliminary Specification
ACL Products	

74AC/ACT11470

Octal transceiver/register with dual enable (3-State)

FEATURES

- Combines '245 and '374 type functions in one chip
- 8-bit octal transceiver with D-type flip-flops
- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11470 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11470 Octal Transceiver/Register contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. Dual Enable ($\overline{E}_{AB}$, $\overline{E}_{BA}$) and Output Enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP_{XX} to A_n or B_n	C_L = 50pF		5.3	7.1	ns
C_{PD}	Power dissipation capacitance per register[1]	f = 1MHz; C_L = 50pF	Enabled	38	41	pF
			Disabled	23	27	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12.0	12.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF		135	125	MHz

Note:

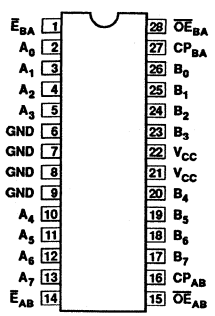
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

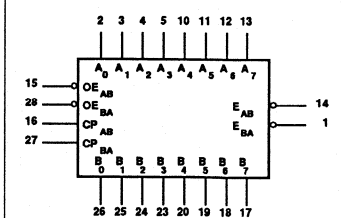
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11470N 74ACT11470N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11470D 74ACT11470D

PIN CONFIGURATION

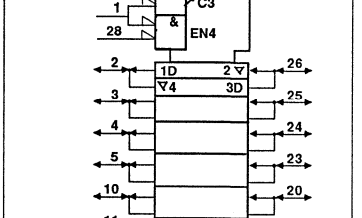
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver/register with dual enable (3-State)

74AC/ACT11470

PIN DESCRIPTION

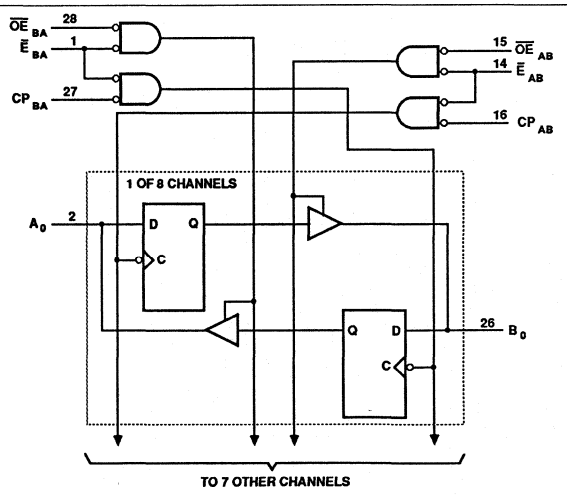
PIN NUMBER	SYMBOL	NAME AND FUNCTION
16	CP_{AB}	A-to-B clock input (active Low)
27	CP_{BA}	B-to-A clock input (active Low)
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
14	$\overline{E}_{AB}$	A-to-B enable input (active Low)
1	$\overline{E}_{BA}$	B-to-A enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13	$A_0 - A_7$	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17	$B_0 - B_7$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	CP_{XX}	Data		
H	X	X	X	Z	Outputs disabled
X	H	X	X	Z	Outputs and clock disabled
L	L	↑	l h	L H	Load register
X	↑	L	l h	Z	Load register and disable outputs

H = High voltage level
h = High state present one setup time before the Low-to-High transition
L = Low voltage level
= Low state present one setup time before the Low-to-High transition
↑ = Low-to-High transition
X = Don't care
Z = High-impedance state

LOGIC DIAGRAM



Octal transceiver/register with dual enable (3-State)

74AC/ACT11470

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11470			74ACT11470			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±400	mA
	DC ground current		±400	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal transceiver/register with dual enable (3-State)

74AC/ACT11470

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11470				74ACT11470				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	$V_I = V_{IL}$ or V_{IH}, $V_O = V_{CC}$ or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Octal transceiver/register with dual enable (3-State)

74AC/ACT11470

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11470					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	75	110		75		MHz
t_{PLH} t_{PHL}	Propagaion delay, CP_{BA} to A_n or CP_{AB} to B_n	1	4.1 4.8	7.3 7.8	8.9 9.3	4.1 4.8	9.8 10.2	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to A_n or $\overline{OE}_{AB}$ to B_n	2	4.3 5.3	7.5 8.7	9.2 10.5	4.3 5.3	10.1 11.6	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	2	5.0 6.0	8.2 9.4	9.9 11.2	5.0 6.0	10.8 12.3	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n or $\overline{OE}_{AB}$ to B_n	2	4.0 4.0	6.8 6.8	8.6 8.7	4.0 4.0	9.2 9.1	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	2	4.3 4.4	7.2 7.2	8.9 9.1	4.3 4.4	9.5 9.6	ns
t_S	Setup time, High or Low A_n to CP_{AB} or B_n to CP_{BA}	3	2.0			2.0		ns
t_H	Hold time, High or Low CP_{BA} to A_n or CP_{AB} to B_n	3	1.5			1.5		ns
t_S	Setup time, High or Low A_n to $\overline{E}_{AB}$ or B_n to $\overline{E}_{BA}$	3	2.0			2.0		ns
t_H	Hold time, High or Low $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	3	1.5			1.5		ns
t_W	Clock pulse width High or Low	1	6.5			6.5		ns

Octal transceiver/register with dual enable (3-State)

74AC/ACT11470

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11470					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	130		110		MHz
t_{PLH} t_{PHL}	Propagaion delay, CP_{BA} to A_n or CP_{AB} to B_n	1	2.1 2.7	4.8 5.7	6.4 7.6	2.1 2.7	7.0 8.4	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to A_n or $\overline{OE}_{AB}$ to B_n	2	2.6 3.5	5.1 6.5	6.8 8.6	2.6 3.5	7.4 9.4	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	2	3.1 3.9	5.6 7.0	7.3 9.0	3.1 3.9	8.0 9.8	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n or $\overline{OE}_{AB}$ to B_n	2	3.1 3.2	5.5 5.5	7.2 7.6	3.1 3.2	7.6 7.9	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	2	3.3 3.4	5.6 5.8	7.5 7.7	3.3 3.4	7.9 8.1	ns
t_S	Setup time, High or Low A_n to CP_{AB} or B_n to CP_{BA}	3	1.5			1.5		ns
t_H	Hold time, High or Low CP_{BA} to A_n or CP_{AB} to B_n	3	1.5			1.5		ns
t_S	Setup time, High or Low A_n to $\overline{E}_{AB}$ or B_n to $\overline{E}_{BA}$	3	2.0			2.0		ns
t_H	Hold time, High or Low $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	3	1.0			1.0		ns
t_W	Clock pulse width High or Low	1	4.5			4.5		ns

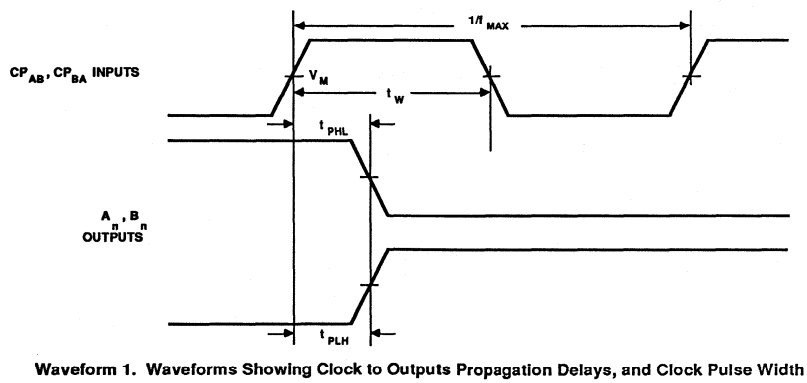
Octal transceiver/register with dual enable (3-State)

74AC/ACT11470

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11470					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	90	120		90		MHz
t_{PLH} t_{PHL}	Propagaion delay, CP_{BA} to A_n or CP_{AB} to B_n	1	3.4 4.2	6.5 7.6	8.3 9.5	3.4 4.2	9.1 10.4	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to A_n or $\overline{OE}_{AB}$ to B_n	2	3.3 4.3	6.3 7.8	8.5 10.3	3.3 4.3	9.2 11.4	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	2	3.4 4.6	6.5 8.1	8.8 10.7	3.4 4.6	9.6 11.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n or $\overline{OE}_{AB}$ to B_n	2	4.8 5.1	7.4 7.3	8.8 8.8	4.8 5.1	9.4 9.3	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	2	5.1 5.1	7.4 7.5	9.1 8.9	5.1 5.1	9.8 9.5	ns
t_S	Setup time, High or Low A_n to CP_{AB} or B_n to CP_{BA}	3	2.0			2.0		ns
t_H	Hold time, High or Low CP_{BA} to A_n or CP_{AB} to B_n	3	3.0			3.0		ns
t_S	Setup time, High or Low A_n to $\overline{E}_{AB}$ or B_n to $\overline{E}_{BA}$	3	2.0			2.0		ns
t_H	Hold time, High or Low $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	3	2.5			2.5		ns
t_W	Clock pulse width High or Low	1	5.5			5.5		ns

AC WAVEFORMS

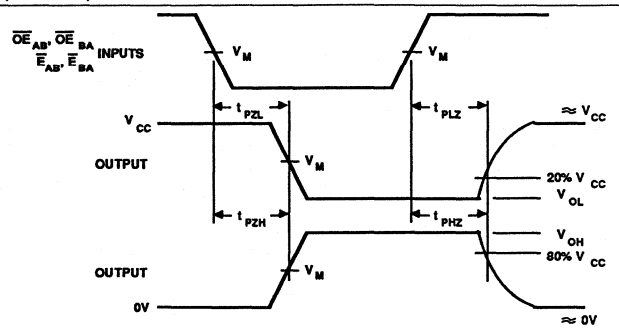


Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays, and Clock Pulse Width

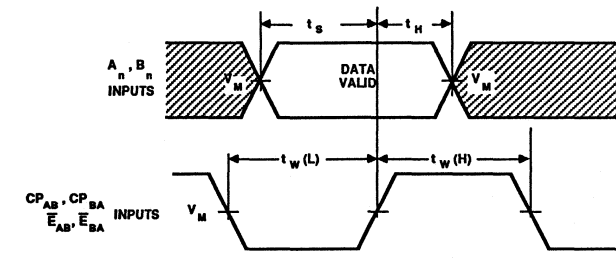
Octal transceiver/register with dual enable (3-State)

74AC/ACT11470

AC WAVEFORMS (Continued)



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

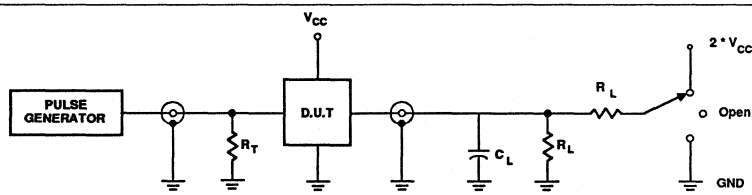


Waveform 3. Waveforms Showing the Data Set-up and Hold Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	August 23, 1990
Status	Preliminary Specification
ACL Products	

74AC/ACT11471

Octal transceiver/register with dual enable, INV (3-State)

FEATURES

- Combines '245 and '374 type functions in one chip
- 8-bit octal transceiver with D-type flip-flops
- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11471 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11471 Octal Transceiver/Register contains two sets of D-type flip-flops for temporary storage of data flowing in either direction. Dual Enable ($\overline{E}_{AB}$, $\overline{E}_{BA}$) and Output Enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP_{XX} to $\overline{A}_n$ or $\overline{B}_n$	C_L = 50pF		5.7	7.1	ns
C_{PD}	Power dissipation capacitance per register[1]	f = 1MHz; C_L = 50pF	Enabled	36	42	pF
			Disabled	23	28	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12.0	12.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF		135	125	MHz

Note:

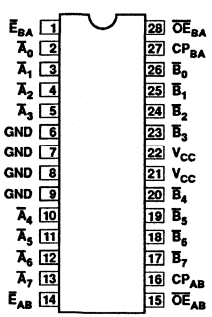
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

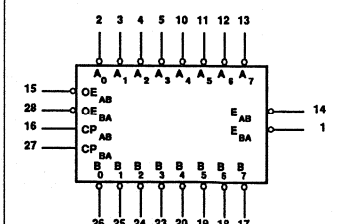
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11471N 74ACT11471N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11471D 74ACT11471D

PIN CONFIGURATION

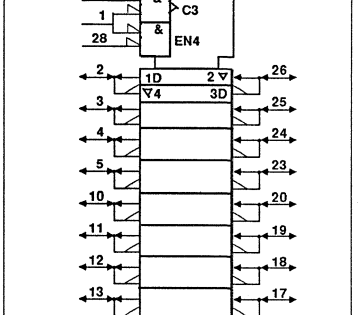
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver/register with dual enable, INV (3-State)

74AC/ACT11471

PIN DESCRIPTION

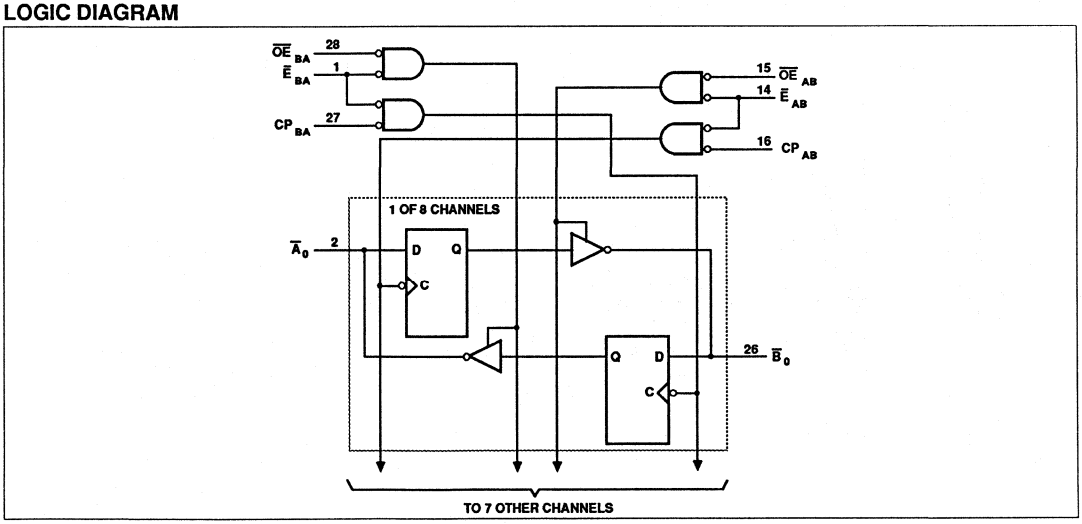
PIN NUMBER	SYMBOL	NAME AND FUNCTION
16	CP_{AB}	A-to-B clock input (active Low)
27	CP_{BA}	B-to-A clock input (active Low)
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
14	$\overline{E}_{AB}$	A-to-B enable input (active Low)
1	$\overline{E}_{BA}$	B-to-A enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0$ - $\overline{A}_7$	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ - $\overline{B}_7$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	CP_{XX}	Data		
H	X	X	X	Z	Outputs disabled
X	H	X	X	Z	Outputs and clock disabled
L	L	↑	l h	H L	Load register
X	↑	L	l h	Z	Load register and disable outputs

H = High voltage level
h = High state present one setup time before the Low-to-High transition
L = Low voltage level
= Low state present one setup time before the Low-to-High transition
↑ = Low-to-High transition
X = Don't care
Z = High-impedance state

LOGIC DIAGRAM



Octal transceiver/register with dual enable, INV (3-State)

74AC/ACT11471

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11471			74ACT11471			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±400	mA
	DC ground current		±400	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal transceiver/register with dual enable, INV (3-State)

74AC/ACT11471

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11471				74ACT11471				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off–state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Octal transceiver/register with dual enable, INV (3-State)

74AC/ACT11471

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11471					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	75	100		75		MHz
t_{PLH} t_{PHL}	Propagaion delay, CP_{BA} to $\overline{A}_n$ or CP_{AB} to $\overline{B}_n$	1	4.7 5.2	7.7 8.3	9.1 9.9	4.7 5.2	10.2 11.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	2	5.1 6.3	8.2 9.6	9.6 11.2	5.1 6.3	10.6 12.6	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	2	5.8 6.9	8.9 10.4	10.4 12.1	5.8 6.9	11.4 13.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	2	4.9 4.9	7.3 7.1	8.8 8.4	4.9 4.9	9.4 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	2	5.2 5.3	7.7 7.7	9.2 9.2	5.2 5.3	9.9 9.8	ns
t_S	Setup time, High or Low $\overline{A}_n$ to CP_{AB} or $\overline{B}_n$ to CP_{BA}	3	1.5			1.5		ns
t_H	Hold time, High or Low CP_{BA} to $\overline{A}_n$ or CP_{AB} to $\overline{B}_n$	3	2.0			2.0		ns
t_S	Setup time, High or Low $\overline{A}_n$ to $\overline{E}_{AB}$ or $\overline{B}_n$ to $\overline{E}_{BA}$	3	2.0			2.0		ns
t_H	Hold time, High or Low $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	2.0			2.0		ns
t_W	Clock pulse width High or Low	1	6.5			6.5		ns

Octal transceiver/register with dual enable, INV (3-State)

74AC/ACT11471

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11471					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	135		110		MHz
t_{PLH} t_{PHL}	Propagaion delay, CP_{BA} to $\overline{A}_n$ or CP_{AB} to $\overline{B}_n$	1	2.6 3.2	5.2 6.1	6.9 8.0	2.6 3.2	7.6 8.8	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	2	2.9 4.1	5.7 7.2	7.2 9.1	2.9 4.1	7.9 10.2	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	2	3.4 4.5	6.1 7.6	7.8 9.7	3.4 4.5	8.6 10.8	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	2	3.6 3.6	5.8 5.7	7.3 7.1	3.6 3.6	7.8 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	2	3.8 3.9	6.0 6.0	7.7 7.7	3.8 3.9	8.2 8.1	ns
t_S	Setup time, High or Low $\overline{A}_n$ to CP_{AB} or $\overline{B}_n$ to CP_{BA}	3	1.5			1.5		ns
t_H	Hold time, High or Low CP_{BA} to $\overline{A}_n$ or CP_{AB} to $\overline{B}_n$	3	1.5			1.5		ns
t_S	Setup time, High or Low $\overline{A}_n$ to $\overline{E}_{AB}$ or $\overline{B}_n$ to $\overline{E}_{BA}$	3	2.0			2.0		ns
t_H	Hold time, High or Low $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	1.5			1.5		ns
t_W	Clock pulse width High or Low	1	4.5			4.5		ns

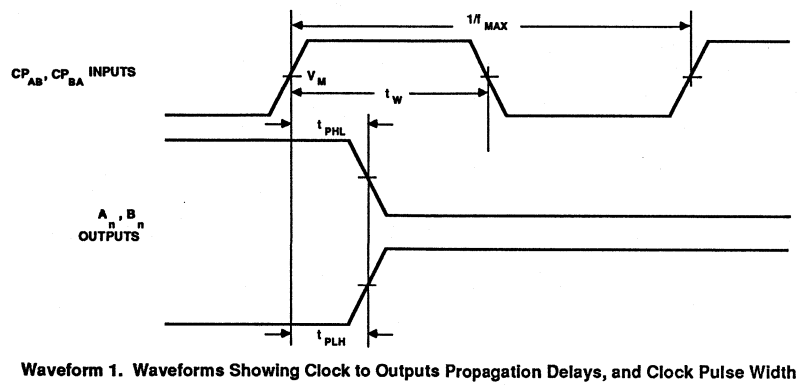
Octal transceiver/register with dual enable, INV (3-State)

74AC/ACT11471

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11471					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	90	125		90		MHz
t_{PLH} t_{PHL}	Propagaion delay, CP_{BA} to $\overline{A}_n$ or CP_{AB} to $\overline{B}_n$	1	4.0 4.5	6.9 7.7	8.5 9.5	4.0 4.5	9.4 10.6	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	2	3.4 4.6	6.6 8.2	9.0 10.8	3.4 4.6	9.9 11.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	2	3.7 4.7	7.0 8.5	9.3 11.2	3.7 4.7	10.3 12.4	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	2	5.0 5.2	7.5 7.5	9.0 8.9	5.0 5.2	9.7 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	2	5.1 5.3	7.6 7.7	9.2 9.3	5.1 5.3	10.0 10.0	ns
t_S	Setup time, High or Low $\overline{A}_n$ to CP_{AB} or $\overline{B}_n$ to CP_{BA}	3	1.5			1.5		ns
t_H	Hold time, High or Low CP_{BA} to $\overline{A}_n$ or CP_{AB} to $\overline{B}_n$	3	2.5			2.5		ns
t_S	Setup time, High or Low $\overline{A}_n$ to $\overline{E}_{AB}$ or $\overline{B}_n$ to $\overline{E}_{BA}$	3	2.0			2.0		ns
t_H	Hold time, High or Low $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	2.5			2.5		ns
t_W	Clock pulse width High or Low	1	5.5			5.5		ns

AC WAVEFORMS

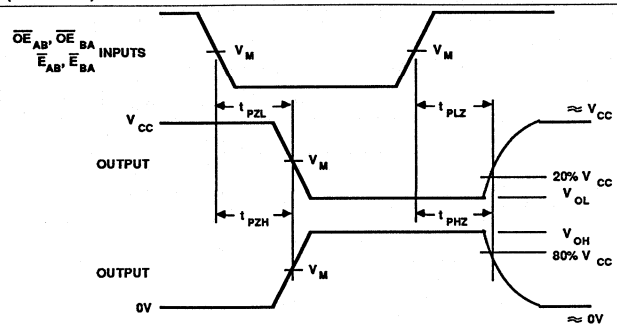


Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays, and Clock Pulse Width

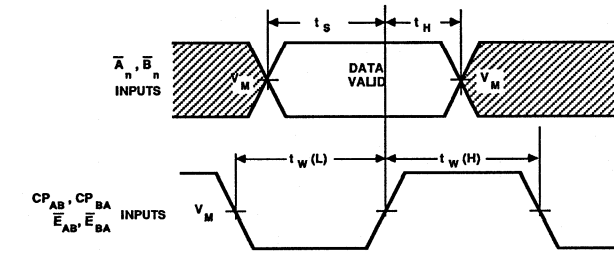
Octal transceiver/register with dual enable, INV (3-State)

74AC/ACT11471

AC WAVEFORMS (Continued)



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

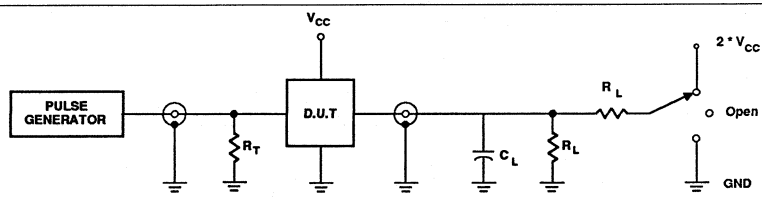


Waveform 3. Waveforms Showing the Data Set-up and Hold Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

AC11543: Preliminary Specification
ACT11543: Product Specification
Octal latched transceiver with dual enable (3-State)

FEATURES

- Combines '245 and '373 type functions in one chip
- 8-bit octal transceiver with D-type latch
- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11543 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11543 Octal Latched Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable (LE_{AB}, LE_{BA}) and Output Enable (OE_{AB}, OE_{BA}) inputs are provided for each register to permit inde-

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	C_L = 50pF		5.5	6.4	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	45	47	pF
			Disabled	10	13	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/Ocapacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

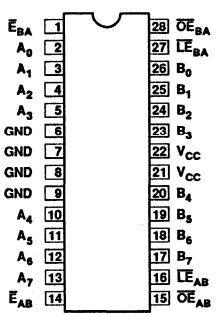
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

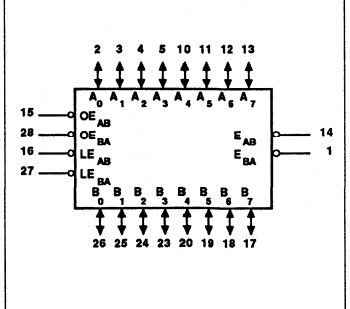
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11543N 74ACT11543N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11543D 74ACT11543D

PIN CONFIGURATION

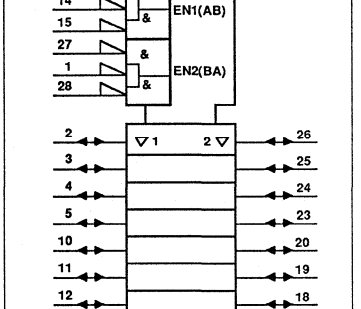
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal latched transceiver with dual enable (3-State)

74AC/ACT11543

pendent control of inputting and outputting in either direction of data flow.

FUNCTIONAL DESCRIPTION

The 74AC/ACT11543 Octal Latched Transceiver contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{E}_{AB}$) input must be Low in order to enter data from A_0 - A_7 or take data from B_0 - B_7 as indicated in the Function Table. With $\overline{E}_{AB}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{LE}_{AB}$) input makes the A-to-B latches transparent; a subsequent Low-to-High transition of the $\overline{LE}_{AB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches. Control of data flow from B to A is similar, but using the $\overline{E}_{BA}$, $\overline{LE}_{BA}$, and $\overline{OE}_{BA}$ inputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
16	$\overline{LE}_{AB}$	A-to-B latch enable input (active Low)
27	$\overline{LE}_{BA}$	B-to-A latch enable input (active Low)
14	$\overline{E}_{AB}$	A-to-B enable input (active Low)
1	$\overline{E}_{BA}$	B-to-A enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13	A_0 - A_7	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17	B_0 - B_7	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

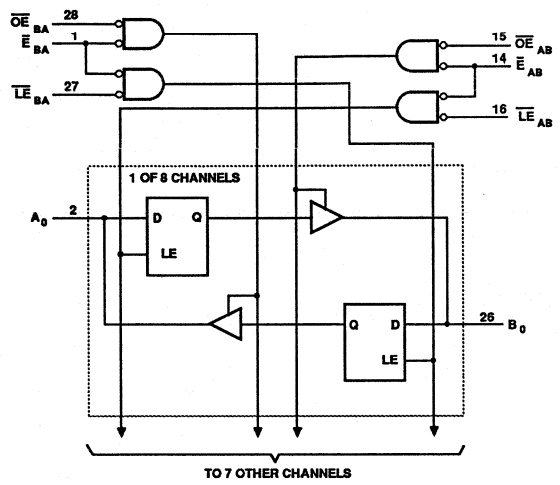
INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	$\overline{LE}_{XX}$	Data		
H	X	X	X	Z	Outputs disabled
X	H	X	X	Z	Outputs disabled
L L	↑ ↑	L L	h l	Z Z	Diasabled + latched
L L	L L	↑ ↑	h l	H L	Latch + display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High state must be present one setup time before the Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)
L = Low voltage level
l = Low state must be present one setup time before the Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)
↑ = Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)
X = Don't care
NC = No change
Z = High-impedance state

Octal latched transceiver with dual enable (3-State)

74AC/ACT11543

LOGIC DIAGRAM



Octal latched transceiver with dual enable (3-State)

74AC/ACT11543

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11543			74ACT11543			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±400	mA
	DC ground current		±400	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal latched transceiver with dual enable (3-State)

74AC/ACT11543

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11543				74ACT11543				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	$V_I = V_{IL}$ or V_{IH}, $V_O = V_{CC}$ or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Octal latched transceiver with dual enable (3-State)

74AC/ACT11543

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11543					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	1	2.9 4.0	7.6 8.8	9.2 10.6	2.9 4.0	10.4 11.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}_{BA}$ to A_n or $\overline{LE}_{AB}$ to B_n	2	3.5 4.3	8.8 9.7	10.7 12.0	3.5 4.3	12.0 13.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to A_n or $\overline{OE}_{AB}$ to B_n	3	3.6 5.2	8.7 10.4	10.4 12.8	3.6 5.2	11.6 15.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	3	4.1 5.7	9.6 11.3	11.4 14.1	4.1 5.7	12.7 16.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n or $\overline{OE}_{AB}$ to B_n	3	3.8 4.0	6.9 6.9	8.6 8.5	3.8 4.0	9.3 9.1	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	3	4.3 4.3	7.7 7.6	9.4 9.8	4.3 4.3	10.1 10.4	ns
t_S	Setup time, High or Low A_n to $\overline{LE}_{AB}$ or B_n to $\overline{LE}_{BA}$	4	3.0			3.0		ns
t_H	Hold time, High or Low $\overline{LE}_{AB}$ to A_n or $\overline{LE}_{BA}$ to B_n	4	0.5			0.5		ns
t_S	Setup time, High or Low A_n to $\overline{E}_{AB}$ or B_n to $\overline{E}_{BA}$	4	3.5			3.5		ns
t_H	Hold time, High or Low $\overline{E}_{AB}$ to A_n or $\overline{E}_{BA}$ to B_n	4	0.0			0.0		ns
t_W	Latch enable pulse width Low	2	400			4.0		ns

Octal latched transceiver with dual enable (3-State)

74AC/ACT11543

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11543					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	1	2.3 3.3	4.8 6.1	6.8 8.0	2.3 3.3	7.5 8.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}_{BA}$ to A_n or $\overline{LE}_{AB}$ to B_n	2	3.0 3.7	5.6 6.6	7.6 8.9	3.0 3.7	8.4 9.9	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to A_n or $\overline{OE}_{AB}$ to B_n	3	3.1 4.4	5.7 7.7	7.6 9.9	3.1 4.4	8.3 11.2	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	3	3.6 4.9	6.2 8.3	8.3 10.6	3.6 4.9	9.1 12.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n or $\overline{OE}_{AB}$ to B_n	3	3.5 3.6	5.5 5.5	7.2 7.3	3.5 3.6	7.7 7.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	3	3.9 4.0	6.0 6.0	7.7 8.1	3.9 4.0	8.3 8.5	ns
t_S	Setup time, High or Low A_n to $\overline{LE}_{AB}$ or B_n to $\overline{LE}_{BA}$	4	2.0			2.0		ns
t_H	Hold time, High or Low $\overline{LE}_{AB}$ to A_n or $\overline{LE}_{BA}$ to B_n	4	1.0			1.0		ns
t_S	Setup time, High or Low A_n to $\overline{E}_{AB}$ or B_n to $\overline{E}_{BA}$	4	2.5			2.5		ns
t_H	Hold time, High or Low $\overline{E}_{AB}$ to A_n or $\overline{E}_{BA}$ to B_n	4	0.5			0.5		ns
t_W	Latch enable pulse width Low	2	4.0			4.0		ns

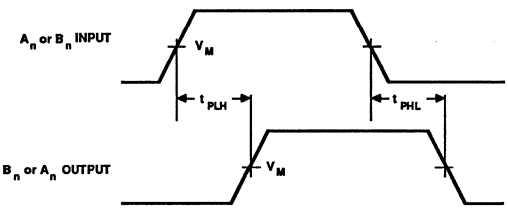
Octal latched transceiver with dual enable (3-State)

74AC/ACT11543

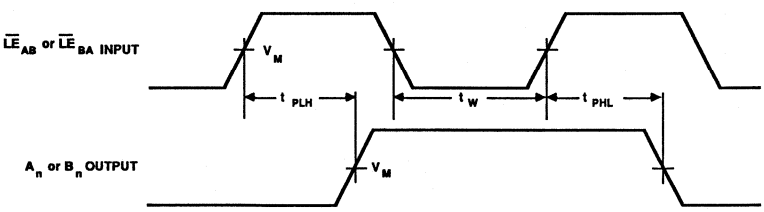
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11543					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	1	3.5 3.2	6.2 6.5	9.1 10.8	3.5 3.2	10.2 12.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}_{BA}$ to A_n or $\overline{LE}_{AB}$ to B_n	2	3.0 3.7	6.1 7.2	10.1 11.7	3.0 3.7	11.2 13.2	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to A_n or $\overline{OE}_{AB}$ to B_n	3	3.3 3.0	6.4 8.0	10.5 12.8	3.3 3.0	11.5 15.3	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	3	3.5 3.2	6.7 8.4	11.1 13.4	3.5 3.2	12.2 16.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n or $\overline{OE}_{AB}$ to B_n	3	4.6 5.0	6.9 7.1	9.6 9.8	4.6 5.0	10.4 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to A_n or $\overline{E}_{AB}$ to B_n	3	4.8 5.1	7.3 7.5	10.1 10.3	4.8 5.1	11.0 11.1	ns
t_S	Setup time, High or Low A_n to $\overline{LE}_{AB}$ or B_n to $\overline{LE}_{BA}$	4	2.5			2.5		ns
t_H	Hold time, High or Low $\overline{LE}_{AB}$ to A_n or $\overline{LE}_{BA}$ to B_n	4	2.0			2.0		ns
t_S	Setup time, High or Low A_n to $\overline{E}_{AB}$ or B_n to $\overline{E}_{BA}$	4	3.0			3.0		ns
t_H	Hold time, High or Low $\overline{E}_{AB}$ to A_n or $\overline{E}_{BA}$ to B_n	4	1.5			1.5		ns
t_W	Latch enable pulse width Low	2	4.0			4.0		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (A_n or B_n) to Output (B_n or A_n) Propagation Delays

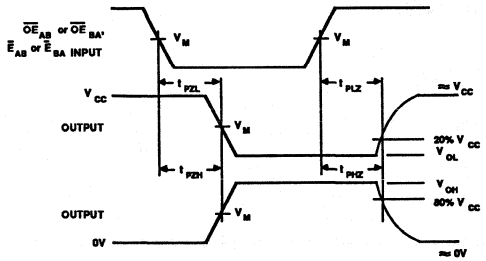


Waveform 2. Waveforms Showing the Latch Enable Input (LE_{XX}) Pulse Width and the Latch Enable Input to Output (A_n or B_n) Propagation Delays

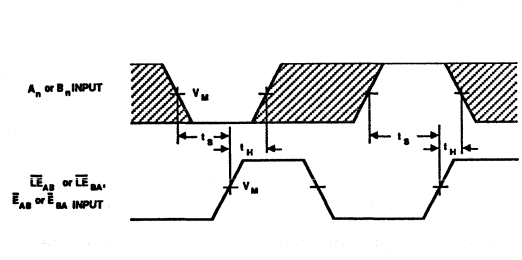
Octal latched transceiver with dual enable (3-State)

74AC/ACT11543

AC WAVEFORMS (Continued)



Waveform 3. Waveforms Showing the 3-State Output Enable and Disable Times

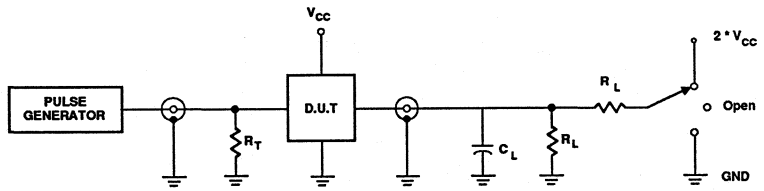


Waveform 4. Waveforms Showing the Data Setup and Hold Times for A_n or B_n Input to Latch Enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and Enable ($\overline{E}_{AB}$, $\overline{E}_{BA}$) Inputs

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

AC11544: Preliminary Specification
ACT11544: Product Specification
Octal latched transceiver with dual enable (3-State), INV

FEATURES

- Combines '245 and '373 type functions in one chip
- 8-bit octal transceiver with D-type latch
- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11544 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11544 Octal Latched Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and Output Enable ($\overline{OE}_{AB}$, $\overline{OE}_{BA}$) inputs are provided for each register to permit inde-

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to $\overline{B}_n$ or B_n to $\overline{A}_n$	C_L = 50pF		5.4	6.5	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	43	47	pF
			Disabled	12	14	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

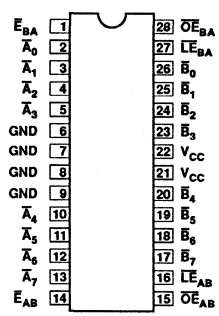
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

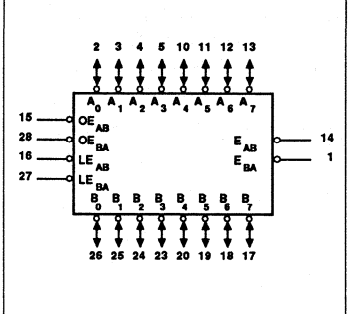
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11544N 74ACT11544N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11544D 74ACT11544D

PIN CONFIGURATION

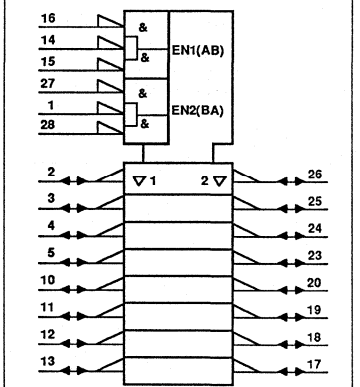
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

pendent control of inputting and outputting in either direction of data flow.

FUNCTIONAL DESCRIPTION

The 74AC/ACT11543 Octal Latched Transceiver contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{E}_{AB}$) input must be Low in order to enter data from A_0 - A_7 or take data from B_0 - B_7 as indicated in the Function Table. With $\overline{E}_{AB}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{LE}_{AB}$) input makes the A-to-B latches transparent; a subsequent Low-to-High transition of the $\overline{LE}_{AB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{E}_{AB}$ and $\overline{OE}_{AB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches. Control of data flow from B to A is similar, but using the $\overline{E}_{BA}$, $\overline{LE}_{BA}$, and $\overline{OE}_{BA}$ inputs.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	$\overline{OE}_{AB}$	A-to-B output enable input (active Low)
28	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
16	$\overline{LE}_{AB}$	A-to-B latch enable input (active Low)
27	$\overline{LE}_{BA}$	B-to-A latch enable input (active Low)
14	$\overline{E}_{AB}$	A-to-B enable input (active Low)
1	$\overline{E}_{BA}$	B-to-A enable input (active Low)
2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0$ - $\overline{A}_7$	Data inputs/outputs (A side)
26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ - $\overline{B}_7$	Data inputs/outputs (B side)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

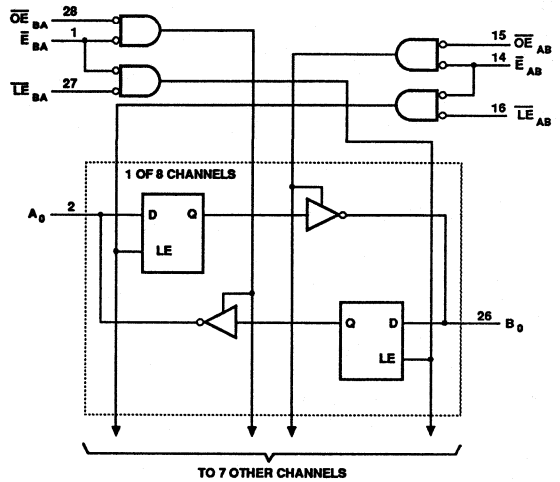
INPUTS				OUTPUTS	STATUS
$\overline{OE}_{XX}$	$\overline{E}_{XX}$	$\overline{LE}_{XX}$	Data		
H	X	X	X	Z	Outputs disabled
X	H	X	X	Z	Outputs disabled
L L	↑ ↑	L L	h l	Z Z	Diasabled + latched
L L	L L	↑ ↑	h l	L H	Latch + display
L L	L L	L L	H L	L H	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High state must be present one setup time before the Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)
L = Low voltage level
l = Low state must be present one setup time before the Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)
↑ = Low-to-High transition of $\overline{LE}_{XX}$ or $\overline{E}_{XX}$ (XX = AB or BA)
X = Don't care
NC = No change
Z = High-impedance state

Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

LOGIC DIAGRAM



Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11544			74ACT11544			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±400	mA
	DC ground current		±400	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11544				74ACT11544				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off–state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11544					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$ or B_n to $\overline{A}_n$	1	2.9 3.7	7.4 7.9	8.9 9.5	2.9 3.7	10.0 10.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}_{BA}$ to $\overline{A}_n$ or $\overline{LE}_{AB}$ to $\overline{B}_n$	2	3.4 4.5	8.3 9.4	9.7 11.0	3.4 4.5	10.9 12.3	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	3	3.4 4.7	8.2 9.6	9.8 11.2	3.4 4.7	10.9 12.7	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	4.2 5.4	9.2 10.6	10.8 12.3	4.2 5.4	12.1 13.8	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	3	4.0 3.9	7.3 7.1	9.0 8.6	4.0 3.9	9.7 9.2	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	4.4 4.8	8.1 8.1	9.9 9.6	4.4 4.8	10.7 10.3	ns
t_S	Setup time, High or Low A_n to $\overline{LE}_{AB}$ or B_n to $\overline{LE}_{BA}$	4	3.0			3.0		ns
t_H	Hold time, High or Low $\overline{LE}_{AB}$ to $\overline{A}_n$ or $\overline{LE}_{BA}$ to $\overline{B}_n$	4	0.5			0.5		ns
t_S	Setup time, High or Low A_n to $\overline{E}_{AB}$ or B_n to $\overline{E}_{BA}$	4	4.0			4.0		ns
t_H	Hold time, High or Low $\overline{E}_{AB}$ to $\overline{A}_n$ or $\overline{E}_{BA}$ to $\overline{B}_n$	4	0.0			0.0		ns
t_W	Latch enable pulse width Low	2	4.0			4.0		ns

Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11544					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$ or B_n to $\overline{A}_n$	1	2.6 3.0	4.9 5.8	6.7 7.8	2.6 3.0	7.4 8.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}_{BA}$ to $\overline{A}_n$ or $\overline{LE}_{AB}$ to $\overline{B}_n$	2	3.0 3.9	5.4 6.8	7.2 8.6	3.0 3.9	8.0 9.6	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	3	3.1 4.0	5.6 7.1	7.4 9.2	3.1 4.0	8.2 10.3	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	3.7 4.7	6.3 7.8	8.2 9.8	3.7 4.7	9.1 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	3	3.6 3.6	5.8 5.7	7.5 7.6	3.6 3.6	8.0 8.1	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	4.1 4.4	6.4 6.4	8.2 8.0	4.1 4.4	8.8 8.5	ns
t_S	Setup time, High or Low A_n to $\overline{LE}_{AB}$ or B_n to $\overline{LE}_{BA}$	4	2.5			2.5		ns
t_H	Hold time, High or Low $\overline{LE}_{AB}$ to $\overline{A}_n$ or $\overline{LE}_{BA}$ to $\overline{B}_n$	4	1.0			1.0		ns
t_S	Setup time, High or Low A_n to $\overline{E}_{AB}$ or B_n to $\overline{E}_{BA}$	4	3.0			3.0		ns
t_H	Hold time, High or Low $\overline{E}_{AB}$ to $\overline{A}_n$ or $\overline{E}_{BA}$ to $\overline{B}_n$	4	0.5			0.5		ns
t_W	Latch enable pulse width Low	2	4.0			4.0		ns

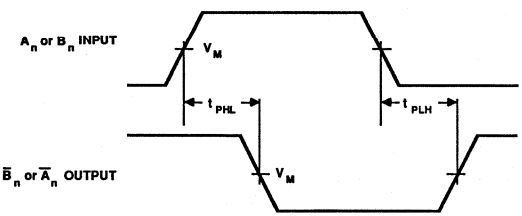
Octal latched transceiver with dual enable (3-State), INV

74AC/ACT11544

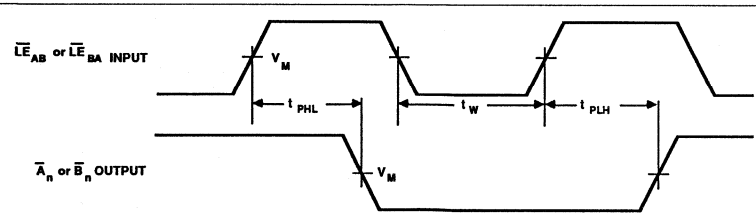
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11544					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$ or B_n to $\overline{A}_n$	1	2.4 4.1	5.7 7.3	8.2 9.3	2.4 4.1	8.9 10.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}_{BA}$ to $\overline{A}_n$ or $\overline{LE}_{AB}$ to $\overline{B}_n$	2	2.6 3.4	6.0 7.1	8.7 10.1	2.6 3.4	9.5 11.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	3	3.0 3.5	6.4 7.8	9.0 10.8	3.0 3.5	9.9 12.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	3.3 3.6	6.7 8.2	9.5 11.2	3.3 3.6	10.4 13.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$ or $\overline{OE}_{AB}$ to $\overline{B}_n$	3	4.6 4.6	7.3 7.2	9.3 9.2	4.6 4.6	9.9 9.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{E}_{BA}$ to $\overline{A}_n$ or $\overline{E}_{AB}$ to $\overline{B}_n$	3	4.8 4.7	7.6 7.6	9.7 9.5	4.8 4.7	10.4 10.2	ns
t_S	Setup time, High or Low A_n to $\overline{LE}_{AB}$ or B_n to $\overline{LE}_{BA}$	4	2.5			2.5		ns
t_H	Hold time, High or Low $\overline{LE}_{AB}$ to $\overline{A}_n$ or $\overline{LE}_{BA}$ to $\overline{B}_n$	4	2.0			2.0		ns
t_S	Setup time, High or Low A_n to $\overline{E}_{AB}$ or B_n to $\overline{E}_{BA}$	4	3.0			3.0		ns
t_H	Hold time, High or Low $\overline{E}_{AB}$ to $\overline{A}_n$ or $\overline{E}_{BA}$ to $\overline{B}_n$	4	1.5			1.5		ns
t_W	Latch enable pulse width Low	2	4.0			4.0		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (A_n or B_n) to Output ($\overline{B}_n$ or $\overline{A}_n$) Propagation Delays



Waveform 2. Waveforms Showing the Latch Enable Input (LE_{XX}) Pulse Width and the Latch Enable Input to Output ($\overline{A}_n$ or $\overline{B}_n$) Propagation Delays

Octal latched transceiver with dual enable (3-State), INV

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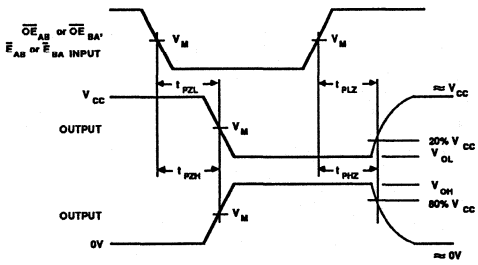
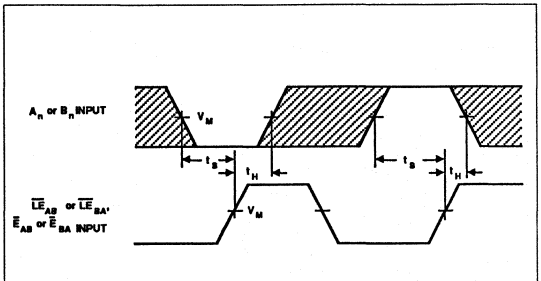
AC WAVEFORMS (Continued)



Waveform 3. Waveforms Showing the 3-State Output Enable and Disable Times

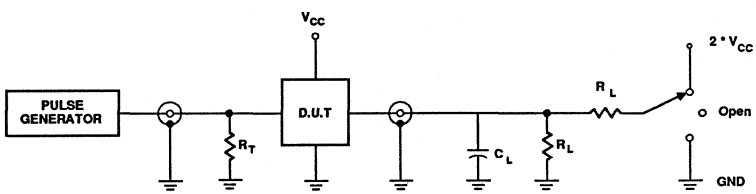


Waveform 4. Waveforms Showing the Data Setup and Hold Times for A_n or B_n Input to Latch Enable ($\overline{LE}_{AB}$, $\overline{LE}_{BA}$) and Enable ($\overline{E}_{AB}$, $\overline{E}_{BA}$) Inputs

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11620

Octal transceiver with dual enable (3-State), INV

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Inverting version of '623
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11620 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11620 device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		5.0	5.8	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	54	54	pF
			Disabled	11	11	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{IO}	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

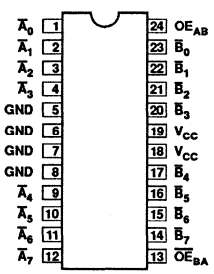
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

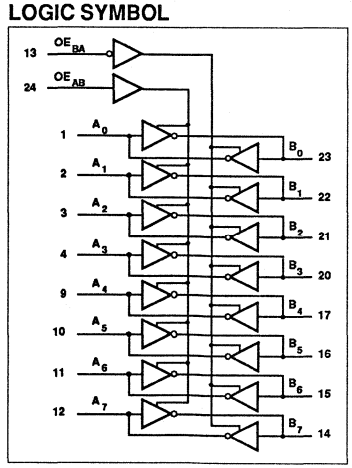
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11620N 74ACT11620N
24-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11620D 74ACT11620D

PIN CONFIGURATION

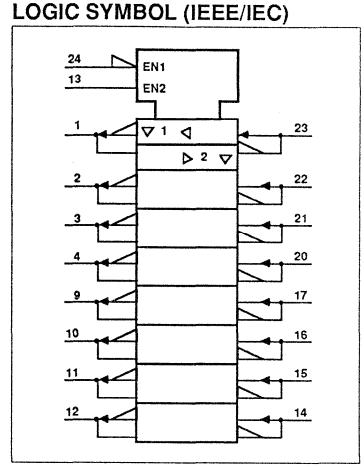
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver with dual enable (3-State), INV — 74AC/ACT11620

control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs (OE_{AB}, $\overline{OE}_{BA}$). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives this transceiver the capability to store data by the simultaneous enabling of OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	OE_{AB}	3-state output enable (active High)
13	$\overline{OE}_{BA}$	3-state output enable (active Low)
1, 2,3, 4, 9, 10, 11, 12	A_0 - A_7	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	B_0 - B_7	Data inputs/outputs (B side)
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE INPUTS		OPERATION
OE_{AB}	$\overline{OE}_{BA}$	
L	L	B data to $\overline{A}$ bus
H	H	A data to $\overline{B}$ bus
L	H	Z
H	L	B data to $\overline{A}$ bus, A data to $\overline{B}$ bus

H = High voltage level
L = Low volatge level
Z = High-impedance (OFF) state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11620			74ACT11620			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	A or B	0		10	0		10	ns/V
		$\overline{OE}_{BA}$ or OE_{AB}	0		5	0		5	
T_{amb}	Operating free-air temperature range		-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal transceiver with dual enable (3-State), INV — 74AC/ACT11620

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11620				74ACT11620				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Octal transceiver with dual enable (3-State), INV — 74AC/ACT11620

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11620					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$	1	1.5 1.5	6.8 6.5	9.0 8.2	1.5 1.5	11.1 9.8	ns
t_{PLH} t_{PHL}	Propagation delay B_n to $\overline{A}_n$	1	1.5 1.5	6.8 6.5	9.0 8.2	1.5 1.5	11.1 9.8	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$	2	1.5 1.5	8.0 7.3	10.3 9.8	1.5 1.5	12.7 11.6	ns
t_{PZH} t_{PZL}	Output enable time OE_{AB} to $\overline{B}_n$	2	1.5 1.5	8.4 8.1	10.0 10.1	1.5 1.5	12.4 12.3	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$	2	1.5 1.5	6.7 7.8	8.4 9.6	1.5 1.5	9.5 11.0	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to $\overline{B}_n$	2	1.5 1.5	7.0 7.7	8.7 9.6	1.5 1.5	9.8 10.9	ns

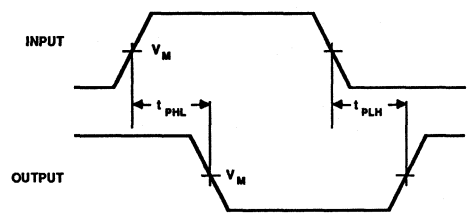
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11620					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$	1	1.5 1.5	5.2 4.8	6.6 6.3	1.5 1.5	7.9 7.7	ns
t_{PLH} t_{PHL}	Propagation delay B_n to $\overline{A}_n$	1	1.5 1.5	5.2 4.8	6.6 6.3	1.5 1.5	7.9 7.7	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$	2	1.5 1.5	6.0 5.5	7.8 7.6	1.5 1.5	9.6 9.2	ns
t_{PZH} t_{PZL}	Output enable time OE_{AB} to $\overline{B}_n$	2	1.5 1.5	6.2 6.0	7.7 7.8	1.5 1.5	9.5 9.6	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$	2	1.5 1.5	5.9 6.3	7.5 8.1	1.5 1.5	8.4 9.2	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to $\overline{B}_n$	2	1.5 1.5	6.1 6.2	7.7 7.9	1.5 1.5	8.5 9.0	ns

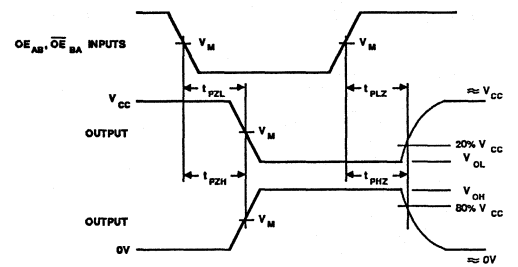
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11620					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$	1	1.5 1.5	5.7 5.9	8.5 7.7	1.5 1.5	10.0 9.2	ns
t_{PLH} t_{PHL}	Propagation delay B_n to $\overline{A}_n$	1	1.5 1.5	5.7 5.9	8.5 7.7	1.5 1.5	10.0 9.2	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to $\overline{A}_n$	2	1.5 1.5	7.2 7.1	9.1 9.2	1.5 1.5	11.1 10.8	ns
t_{PZH} t_{PZL}	Output enable time OE_{AB} to $\overline{B}_n$	2	1.5 1.5	7.5 7.7	10.2 9.8	1.5 1.5	12.2 11.9	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to $\overline{A}_n$	2	1.5 1.5	7.9 8.3	9.6 10.0	1.5 1.5	11.0 11.6	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to $\overline{B}_n$	2	1.5 1.5	7.2 7.2	8.9 8.9	1.5 1.5	9.8 10.0	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input to Output Propagation Delays

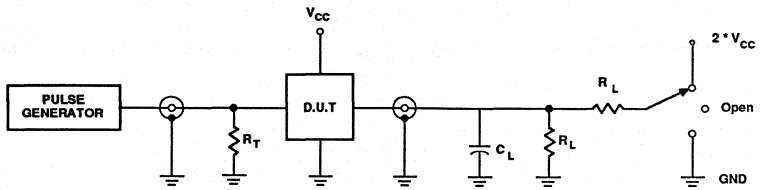


Waveform 2. Waveforms Showing the 3-State Output Enables (OE_{AB}, $\overline{OE}_{BA}$) and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2*V_{CC}$
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11623

Octal transceiver with dual enable (3-State)

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Non-inverting version of '620
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11623 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11623 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		4.8	5.8	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz;	Enabled	49	41	pF
		C_L = 50pF	Disabled	9	8	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
C_{IO}	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

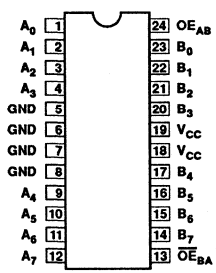
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

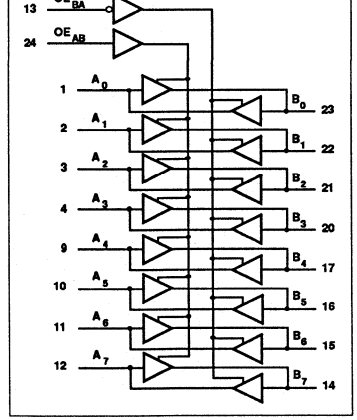
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11623N 74ACT11623N
24-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11623D 74ACT11623D

PIN CONFIGURATION

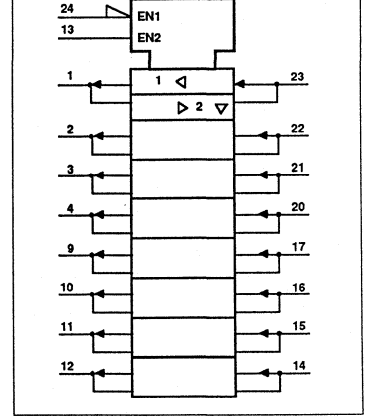
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver with dual enable (3-State)

74AC/ACT11623

control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs (OE_{AB}, $\overline{OE}_{BA}$). The Enable inputs can be used to disable the devices so that the buses are effectively isolated.

The dual-enable configuration gives these transceivers the capability to store data by the simultaneous enabling of OE_{AB} and $\overline{OE}_{BA}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	OE_{AB}	3-state output enable (active High)
13	$\overline{OE}_{BA}$	3-state output enable (active Low)
1, 2,3, 4, 9, 10, 11, 12	A_0 - A_7	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	B_0 - B_7	Data inputs/outputs (B side)
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

ENABLE INPUTS		OPERATION
OE_{AB}	$\overline{OE}_{BA}$	
L	L	B data to A bus
H	H	A data to B bus
L	H	Z
H	L	B data to A bus, A data to B bus

H = High voltage level
L = Low volatge level
Z = High-impedance (OFF) state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11623			74ACT11623			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11623				74ACT11623				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	$V_I = V_{IL}$ or V_{IH}, $V_O = V_{CC}$ or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11623					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	1	1.5 1.5	6.8 6.3	9.2 8.2	1.5 1.5	11.4 10.6	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	1	1.5 1.5	6.8 6.3	9.2 8.2	1.5 1.5	11.4 10.6	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to A_n	2	1.5 1.5	8.0 7.9	10.6 10.4	1.5 1.5	13.3 12.5	ns
t_{PZH} t_{PZL}	Output enable time OE_{AB} to B_n	2	1.5 1.5	8.2 8.3	10.4 10.8	1.5 1.5	13.2 13.2	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n	2	1.5 1.5	7.0 8.0	8.7 9.9	1.5 1.5	9.7 11.3	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to B_n	2	1.5 1.5	7.0 8.0	8.8 9.9	1.5 1.5	9.8 11.1	ns

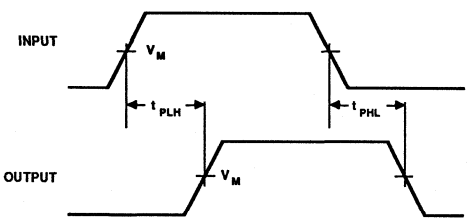
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11623					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	1	1.5 1.5	4.9 4.6	6.8 6.4	1.5 1.5	8.4 7.7	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	1	1.5 1.5	4.9 4.6	6.8 6.4	1.5 1.5	8.4 7.7	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to A_n	2	1.5 1.5	5.8 5.9	7.9 8.1	1.5 1.5	9.8 9.9	ns
t_{PZH} t_{PZL}	Output enable time OE_{AB} to B_n	2	1.5 1.5	6.2 6.1	8.0 8.3	1.5 1.5	10.0 10.2	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n	2	1.5 1.5	6.1 6.6	7.7 8.2	1.5 1.5	8.6 9.3	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to B_n	2	1.5 1.5	6.2 6.5	7.8 8.1	1.5 1.5	8.7 9.2	ns

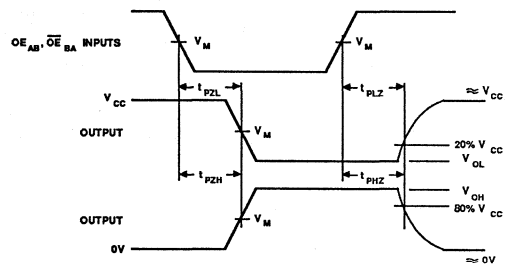
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11623					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	1	1.5 1.5	6.0 5.5	7.5 7.2	1.5 1.5	9.1 8.4	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	1	1.5 1.5	6.0 5.5	7.5 7.2	1.5 1.5	9.1 8.4	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}_{BA}$ to A_n	2	1.5 1.5	6.9 6.9	8.6 9.0	1.5 1.5	10.4 10.6	ns
t_{PZH} t_{PZL}	Output enable time OE_{AB} to B_n	2	1.5 1.5	7.7 7.7	9.3 9.7	1.5 1.5	11.5 11.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n	2	1.5 1.5	8.1 8.5	10.0 10.5	1.5 1.5	11.4 12.2	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to B_n	2	1.5 1.5	7.1 7.3	8.8 9.2	1.5 1.5	9.8 10.4	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input to Output Propagation Delays

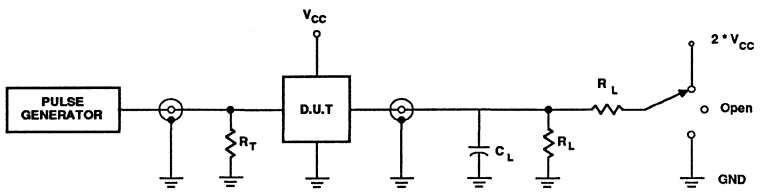


Waveform 2. Waveforms Showing the 3-State Output Enables (OE_{AB}, $\overline{OE}_{BA}$) and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

74AC/ACT11643

Octal transceiver (3-State) True/INV

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11643 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11643 devices are octal transceivers featuring 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The devices feature an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control. Note that data transmitted from the A side to the B side is inverted and that data transmitted from the B side to the A side is not inverted.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		5.2	5.7	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	46	41	pF
			Disabled	9.0	9.0	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.0	4.0	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

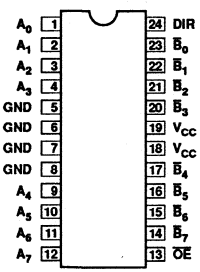
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

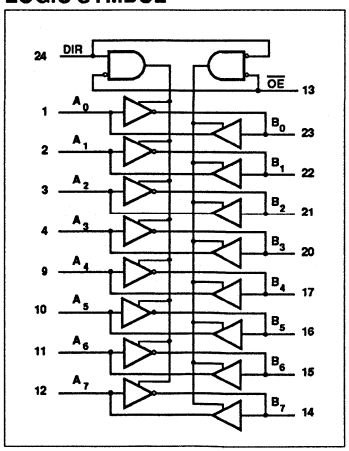
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11643N 74ACT11643N
24-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11643D 74ACT11643D

PIN CONFIGURATION

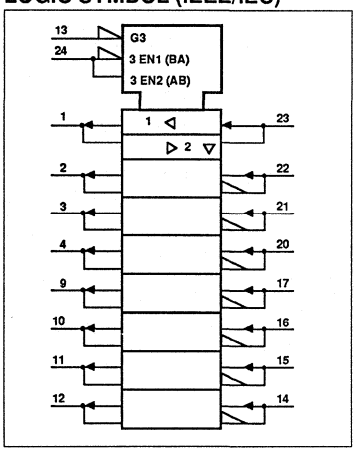
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver (3-State) True/INV — 74AC/ACT11643

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
24	DIR	Direction control input
1, 2, 3, 4, 9, 10, 11, 12	A_0 - A_7	Data inputs/outputs (A side)
23, 22, 21, 20, 17, 16, 15, 14	B_0 - B_7	Data inputs/outputs (B side)
13	$\overline{OE}$	Output enable
5, 6, 7, 8	GND	Ground (0V)
18, 19	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to $\overline{B}$ bus
H	X	Z

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11643			74ACT11643			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal transceiver (3-State) True/INV | 74AC/ACT11643

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11643				74ACT11643				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11643					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$, B_n to A_n	1	1.5 1.5	7.4 6.6	10.1 8.7	1.5 1.5	11.3 10.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	9.4 8.9	11.8 11.4	1.5 1.5	13.3 13.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	8.3 8.9	10.1 10.9	1.5 1.5	10.9 12.0	ns

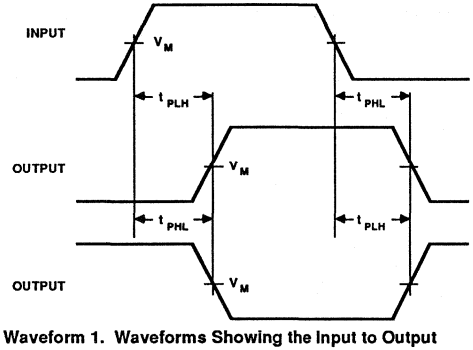
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11643					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$, B_n to A_n	1	1.5 1.5	5.4 5.0	7.7 6.8	1.5 1.5	8.6 7.9	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	7.0 6.6	9.2 8.7	1.5 1.5	10.4 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	7.1 7.2	8.8 9.0	1.5 1.5	9.4 9.8	ns

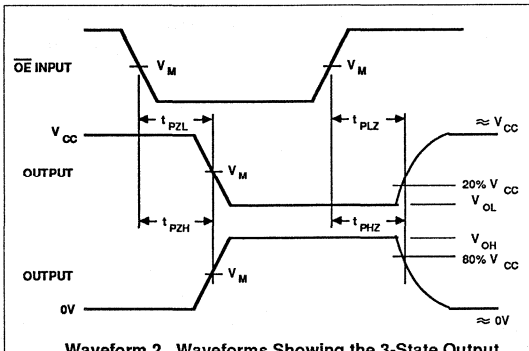
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11643					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{B}_n$, B_n to A_n	1	1.5 1.5	5.6 5.7	8.3 7.7	1.5 1.5	9.3 8.8	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.5 1.5	8.1 7.7	11.5 10.1	1.5 1.5	12.9 11.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.5 1.5	9.1 9.3	12.0 11.6	1.5 1.5	13.1 12.7	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input to Output Propagation Delays

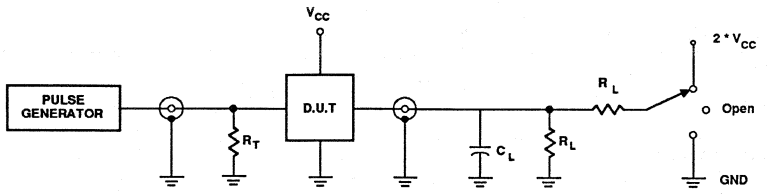


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11646

Octal transceiver/register with direction pin (3-State)

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11646 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11646 device is an octal transceiver/register featuring non-inverting 3-State bus compatible outputs in both send and receive directions, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from internal

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		5.9	7.3	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	59	63	pF
			Disabled	15	14	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{IO}	I/O capacitance	V_O = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP_x to A or B	C_L = 50pF		125	125	MHz

Note:

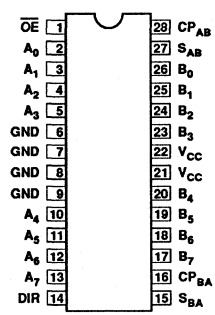
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

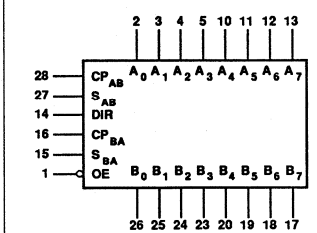
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11646N 74ACT11646N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11646D 74ACT11646D

PIN CONFIGURATION

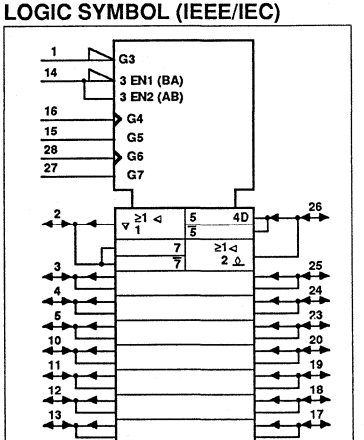
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver/register with direction pin (3-State)

74AC/ACT11646

registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a High logic level. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the High-impedance port may be stored in either the A or B register or both.

The Select inputs (S_X) can multiplex stored and real-time (transparent mode) data. The DIR input determines which bus will receive data when the Output Enable is active (Low). In the isolation mode ($\overline{OE}$ is High), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. Figure 1 demonstrates the four fundamental bus-management functions that can be performed.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
28	CP_{AB}	A-to-B clock input
16	CP_{BA}	B-to-A clock input
27	S_{AB}	A-to-B select input
15	S_{BA}	B-to-A select input
14	DIR	Data flow directional control input
2, 3, 4, 5, 10, 11, 12, 13	A_0 - A_7	A side inputs/outputs (3-state)
26, 25, 24, 23, 20, 19, 18, 17	B_0 - B_7	B side inputs/outputs (3-state)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

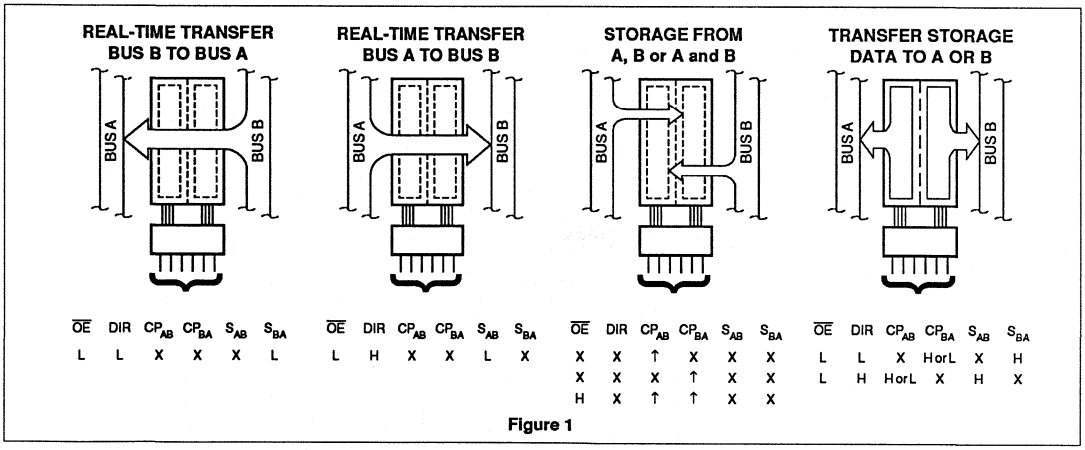


Figure 1

Octal transceiver/register with direction pin (3-State)

74AC/ACT11646

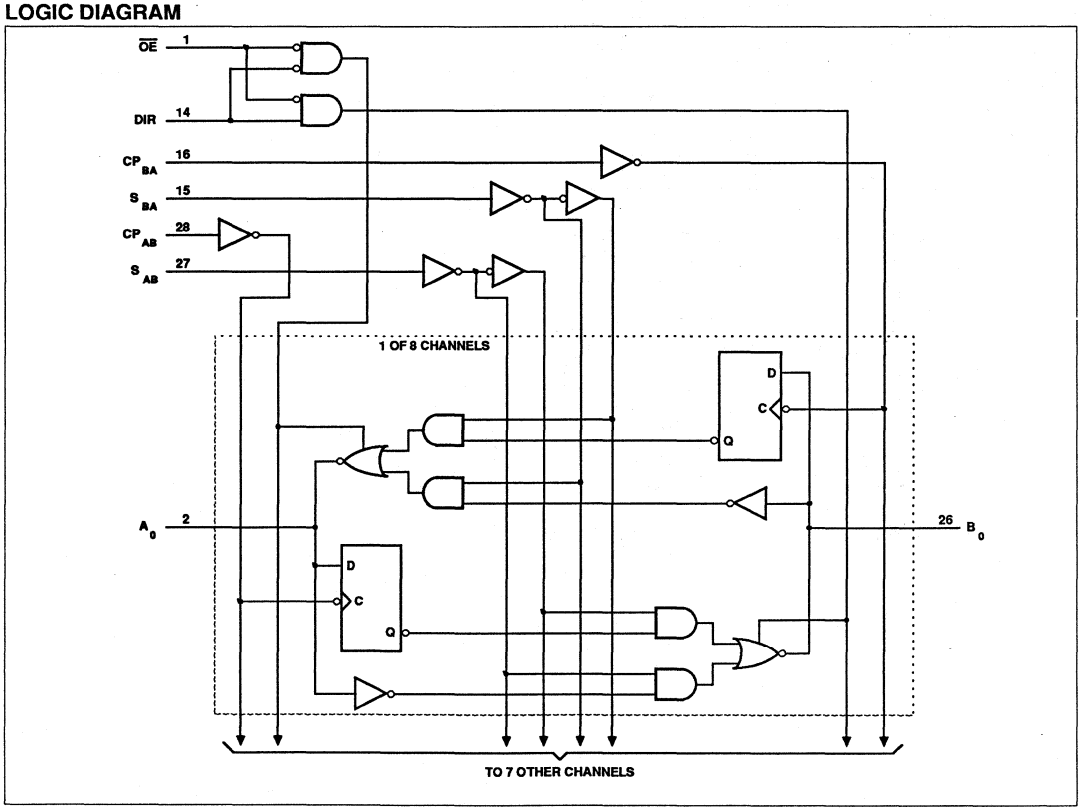
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATING MODE
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 - A_7	B_0 - B_7	
X	X	↑	X	X	X	Input	un*	Store A, B unspecified*
X	X	X	↑	X	X	un*	Input	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B Data Isolation,
H	X	H or L	H or L	X	X			hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus
L	H	H or L	X	H	X			Stored A data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ ad DIR inputs. Data input functions are always enabled, i.e, data at the bus pins will be stored on every Low-to-High transition of the clock.

un = unspecified
H = Highvoltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



Octal transceiver/register with direction pin (3-State)

74AC/ACT11646

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11646			74ACT11646			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal transceiver/register with direction pin (3-State)

74AC/ACT11646

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11646				74ACT11646				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11646					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	65	80		65		MHz
t_{PLH} t_{PHL}	Propagation delay CP_{AB} or CP_{BA} to A_n or B_n	1	1.5 1.5	11.8 13.7	15.0 16.8	1.5 1.5	17.0 18.3	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	3	1.5 1.5	9.1 10.7	12.1 13.4	1.5 1.5	13.8 14.5	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n High) S_{BA} or S_{AB} to A_n or B_n	2	1.5 1.5	9.8 12.0	12.9 14.5	1.5 1.5	14.4 15.8	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n Low) S_{BA} or S_{AB} to A_n or B_n	3	1.5 1.5	10.7 12.4	13.8 15.0	1.5 1.5	15.4 16.4	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	5	1.5 1.5	13.0 16.1	16.4 20.4	1.5 1.5	18.7 21.8	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	5	1.5 1.5	13.7 16.8	17.1 21.0	1.5 1.5	19.4 23.6	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to A_n or B_n	5	1.5 1.5	7.9 7.2	9.6 8.9	1.5 1.5	10.3 9.6	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to A_n or B_n	5	1.5 1.5	7.9 7.3	9.7 9.1	1.5 1.5	10.5 9.9	ns
t_s	Setup time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	6.5			6.5		ns
t_h	Hold time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	1.0			1.0		ns
t_w	Pulse width (High or Low) CP_{AB} or CP_{BA}	1	7.7			7.7		ns

Octal transceiver/register with direction pin (3-State)

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AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11646					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_{AB} or CP_{BA} to A_n or B_n	1	1.5 1.5	7.0 8.2	9.7 11.0	1.5 1.5	11.0 12.2	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	3	1.5 1.5	5.5 6.3	7.9 8.9	1.5 1.5	8.8 9.8	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n High) S_{BA} or S_{AB} to A_n or B_n	2	1.5 1.5	5.9 7.2	8.4 9.8	1.5 1.5	9.4 10.7	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n Low) S_{BA} or S_{AB} to A_n or B_n	3	1.5 1.5	6.3 7.3	8.9 9.9	1.5 1.5	9.9 11.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	5	1.5 1.5	7.8 8.5	10.7 11.9	1.5 1.5	12.0 13.1	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	5	1.5 1.5	8.4 9.1	11.2 12.3	1.5 1.5	12.6 13.7	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to A_n or B_n	5	1.5 1.5	5.9 5.9	8.4 7.7	1.5 1.5	8.9 8.3	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to A_n or B_n	5	1.5 1.5	6.3 5.7	8.2 7.5	1.5 1.5	8.7 8.1	ns
t_s	Setup time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	4.5			4.5		ns
t_h	Hold time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	1.0			1.0		ns
t_w	Pulse width (High or Low) CP_{AB} or CP_{BA}	1	5.0			5.0		ns

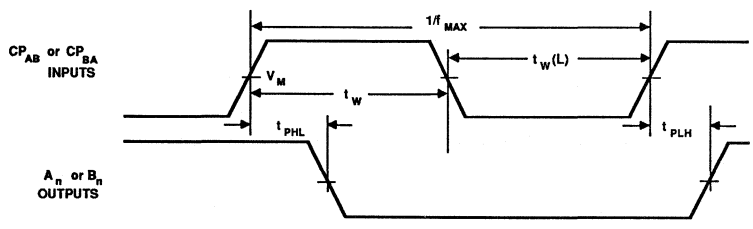
Octal transceiver/register with direction pin (3-State)

74AC/ACT11646

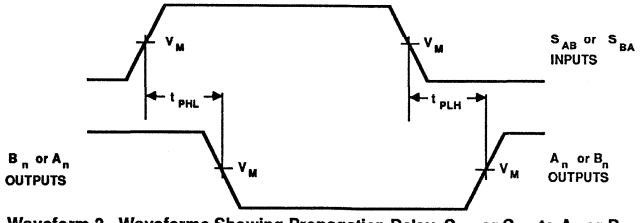
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11646					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_{AB} or CP_{BA} to A_n or B_n	1	1.5 1.5	8.8 10.0	11.9 13.4	1.5 1.5	13.5 14.9	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	3	1.5 1.5	7.3 7.2	10.1 11.0	1.5 1.5	11.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n High) S_{BA} or S_{AB} to A_n or B_n	2	1.5 1.5	6.7 9.1	10.3 12.1	1.5 1.5	11.5 13.5	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n Low) S_{BA} or S_{AB} to A_n or B_n	3	1.5 1.5	8.0 8.1	10.9 11.9	1.5 1.5	12.4 13.1	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	5	1.5 1.5	7.7 9.2	12.8 13.8	1.5 1.5	14.4 15.3	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	5	1.5 1.5	10.2 10.9	13.7 14.8	1.5 1.5	15.3 16.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to A_n or B_n	5	1.5 1.5	8.6 7.8	10.7 9.7	1.5 1.5	11.6 10.6	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to A_n or B_n	5	1.5 1.5	7.9 7.3	10.5 9.5	1.5 1.5	11.3 10.3	ns
t_s	Setup time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	4.5			4.5		ns
t_h	Hold time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	2.5			2.5		ns
t_w	Pulse width (High or Low) CP_{AB} or CP_{BA}	1	5.0			5.0		ns

AC WAVEFORMS

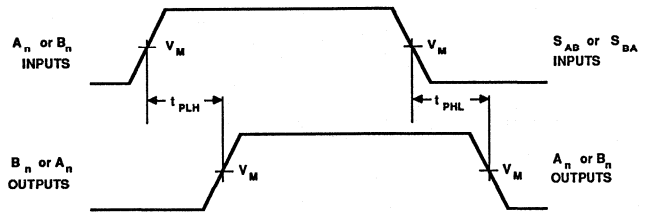


Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width

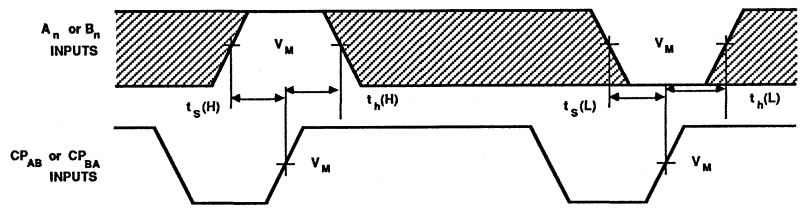


Waveform 2. Waveforms Showing Propagation Delay, S_{BA} or S_{AB} to A_n or B_n

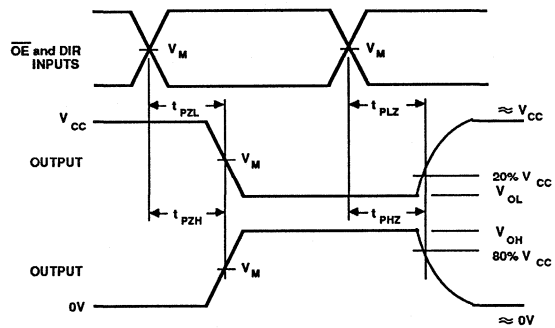
AC WAVEFORMS (Continued)



Waveform 3. Waveforms Showing Propagation Delay, A_n to B_n or B_n to A_n and S_{BA} or S_{AB} to A_n or B_n



Waveform 4. Waveforms Showing the Data Setup and Hold Times



Waveform 5. Waveforms Showing 3-State Output Enable and Disable Times

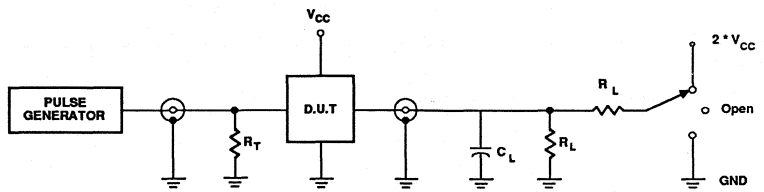
Octal transceiver/register with direction pin (3-State)

74AC/ACT11646

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	August 28, 1990
Status	Preliminary Specification
ACL Products	

74AC/ACT11648

Octal transceiver/register with direction pin (3-State), INV

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11648 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11648 device is an octal transceiver/register featuring inverting 3-State bus compatible outputs in both send and receive directions, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay $\overline{A}_n$ to B_n, or $\overline{B}_n$ to A_n	C_L = 50pF		8.9	10.4	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	65	61	pF
			Disabled	16	15	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{IO}	I/O capacitance	V_O = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP_{XX} to $\overline{A}$ or $\overline{B}$	C_L = 50pF		110	105	MHz

Note:

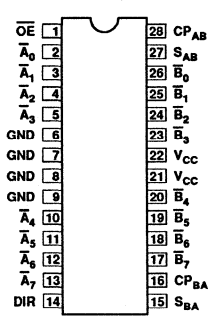
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

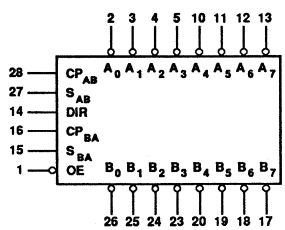
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11648N 74ACT11648N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11648D 74ACT11648D

PIN CONFIGURATION

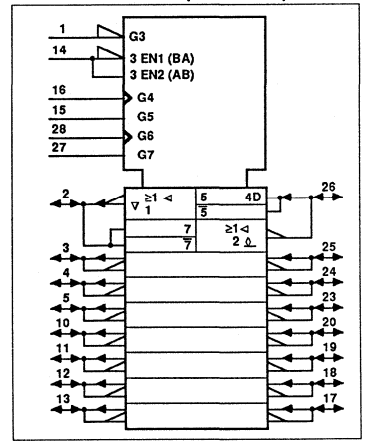
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver/register with direction pin (3-State), INV

74AC/ACT11648

from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a High logic level. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the High-impedance port may be stored in either the A or B register or both.

The Select inputs (S_X) can multiplex stored and real-time (transparent mode) data. The DIR input determines which bus will receive data when the Output Enable is active (Low). In the isolation mode ($\overline{OE}$ is High), A data may be stored in the B register and/or B data may be stored in the A register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time. Figure 1 demonstrates the four fundamental bus-management functions that can be performed.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
28	CP_{AB}	A-to-B clock input
16	CP_{BA}	B-to-A clock input
27	S_{AB}	A-to-B select input
15	S_{BA}	B-to-A select input
14	DIR	Data flow directional control input
2, 3, 4, 5, 10, 11, 12, 13	$\overline{A}_0$ - $\overline{A}_7$	A side inputs/outputs (3-state)
26, 25, 24, 23, 20, 19, 18, 17	$\overline{B}_0$ - $\overline{B}_7$	B side inputs/outputs (3-state)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

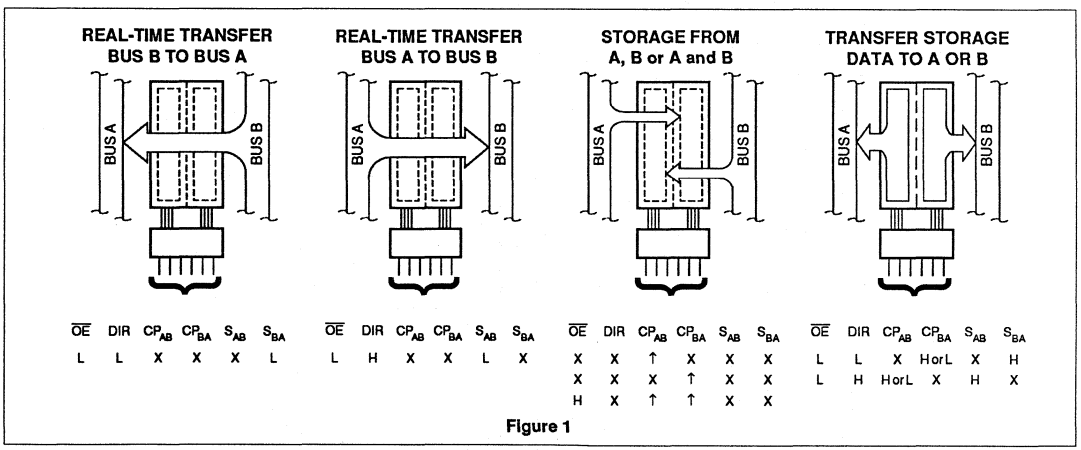


Figure 1

Octal transceiver/register with direction pin (3-State), INV

74AC/ACT11648

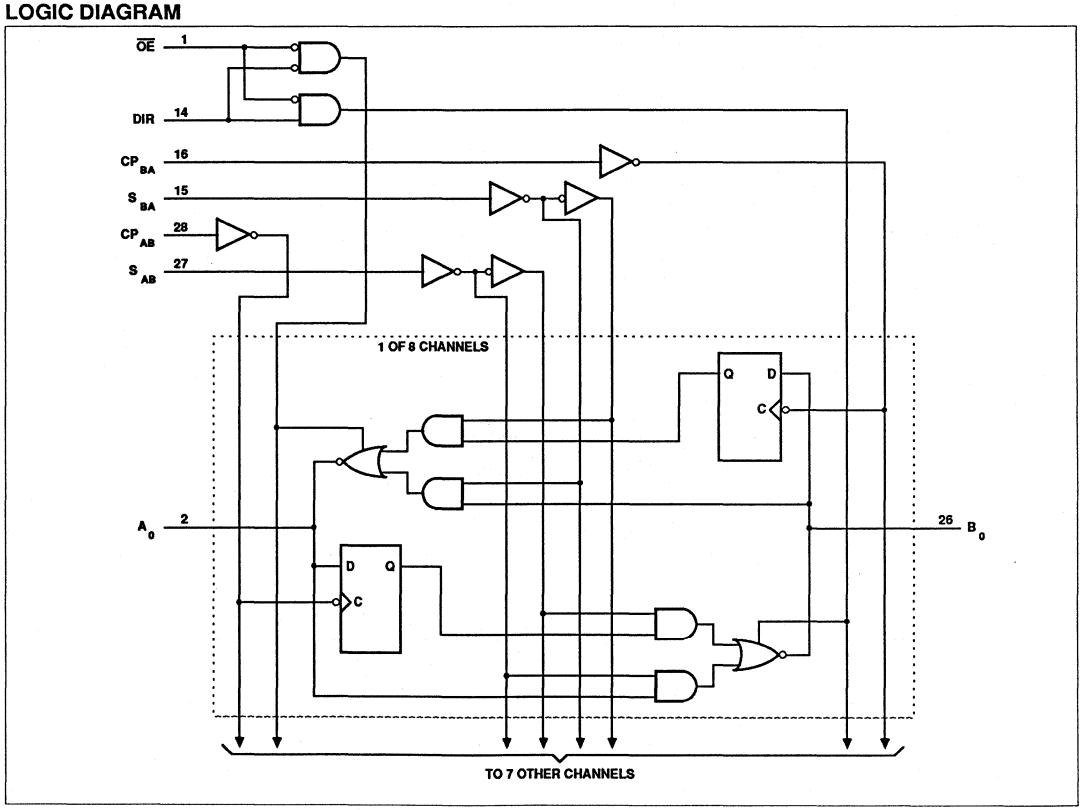
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATING MODE
$\overline{OE}$	DIR	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ - $\overline{A}_7$	$\overline{B}_0$ - $\overline{B}_7$	
X	X	↑	X	X	X	Input	un*	Store A, B unspecified*
X	X	X	↑	X	X	un*	Input	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B Data Isolation,
H	X	H or L	H or L	X	X			hold storage
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			Stored $\overline{A}$ data to B bus

* The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ ad DIR inputs. Data input functions are always enabled, i.e, data at the bus pins will be stored on every Low-to-High transition of the clock.

un = unspecified
H = Highvoltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



Octal transceiver/register with direction pin (3-State), INV

74AC/ACT11648

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11648			74ACT11648			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal transceiver/register with direction pin (3-State), INV

74AC/ACT11648

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11648				74ACT11648				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	$V_I = V_{IL}$ or V_{IH}, $V_O = V_{CC}$ or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Octal transceiver/register with direction pin (3-State), INV

74AC/ACT11648

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11648					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	40	65		40		MHz
t_{PLH} t_{PHL}	Propagation delay CP_{AB} or CP_{BA} to $\overline{A}_n$ or $\overline{B}_n$	1	4.3 5.2	10.1 11.5	15.6 17.6	4.3 5.2	17.6 19.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{B}_n$ or $\overline{A}_n$	3	3.0 3.8	8.7 9.3	12.6 14.4	3.0 3.8	14.3 15.9	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n High) S_{BA} or S_{AB} to $\overline{A}_n$ or $\overline{B}_n$	2	3.7 4.5	9.1 10.3	14.1 15.9	3.7 4.5	15.8 17.4	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n Low) S_{BA} or S_{AB} to $\overline{A}_n$ or $\overline{B}_n$	3	3.2 4.6	8.6 10.3	13.6 15.6	3.2 4.6	15.3 17.1	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to $\overline{A}_n$ or $\overline{B}_n$	5	5.0 5.2	11.1 12.8	17.2 20.5	5.0 5.2	19.4 23.0	ns
t_{PZH} t_{PZL}	Output Enable time DIR to $\overline{A}_n$ or $\overline{B}_n$	5	4.9 5.2	11.6 14.2	18.2 21.6	4.9 5.2	20.6 24.3	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to $\overline{A}_n$ or $\overline{B}_n$	5	4.1 3.7	7.2 6.5	9.9 9.1	4.1 3.7	10.6 9.7	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to $\overline{A}_n$ or $\overline{B}_n$	5	3.8 3.5	7.1 6.5	10.1 9.3	3.8 3.5	10.9 10.1	ns
t_s	Setup time (High or Low) $\overline{A}_n$ or $\overline{B}_n$ to CP_{AB} or CP_{BA}	4	6.5			6.5		ns
t_h	Hold time (High or Low) $\overline{A}_n$ or $\overline{B}_n$ to CP_{AB} or CP_{BA}	4	0.0			0.0		ns
t_w	Pulse width (High or Low) CP_{AB} or CP_{BA}	1	12.5			12.5		ns

Octal transceiver/register with direction pin (3-State), INV

74AC/ACT11648

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11648					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	90	110		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP_{AB} or CP_{BA} to $\overline{A}_n$ or $\overline{B}_n$	1	3.6 4.3	6.9 8.0	10.0 11.4	3.6 4.3	11.4 12.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{B}_n$ or $\overline{A}_n$	3	2.6 3.2	5.6 5.4	8.3 9.4	2.6 3.2	9.5 10.6	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n High) S_{BA} or S_{AB} to $\overline{A}_n$ or $\overline{B}_n$	2	3.1 3.8	6.2 7.6	9.2 10.4	3.1 3.8	10.4 11.6	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n Low) S_{BA} or S_{AB} to $\overline{A}_n$ or $\overline{B}_n$	3	2.8 3.8	6.1 7.3	8.9 10.4	2.8 3.8	10.1 11.6	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to $\overline{A}_n$ or $\overline{B}_n$	5	4.2 4.1	7.8 8.1	11.3 12.0	4.2 4.1	12.8 13.6	ns
t_{PZH} t_{PZL}	Output Enable time DIR to $\overline{A}_n$ or $\overline{B}_n$	5	4.0 4.1	8.0 8.4	11.9 12.7	4.0 4.1	13.4 14.4	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to $\overline{A}_n$ or $\overline{B}_n$	5	3.8 3.5	6.3 5.7	8.6 7.8	3.8 3.5	9.2 8.4	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to $\overline{A}_n$ or $\overline{B}_n$	5	3.5 3.4	6.1 5.9	8.5 7.8	3.5 3.4	9.1 8.4	ns
t_s	Setup time (High or Low) $\overline{A}_n$ or $\overline{B}_n$ to CP_{AB} or CP_{BA}	4	4.5			4.5		ns
t_h	Hold time (High or Low) $\overline{A}_n$ or $\overline{B}_n$ to CP_{AB} or CP_{BA}	4	0.0			0.0		ns
t_w	Pulse width (High or Low) CP_{AB} or CP_{BA}	1	5.6			5.6		ns

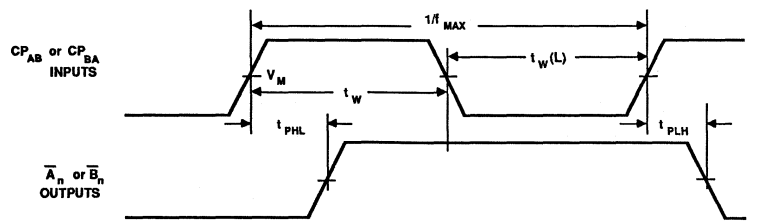
Octal transceiver/register with direction pin (3-State), INV

74AC/ACT11648

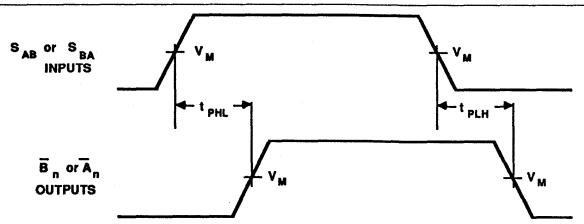
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11648					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	75	105		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP_{AB} or CP_{BA} to $\overline{A}_n$ or $\overline{B}_n$	1	5.2 6.0	9.4 10.5	12.0 13.5	5.2 6.0	13.7 15.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{B}_n$ or $\overline{A}_n$	3	2.4 4.4	6.5 8.5	9.5 11.3	2.4 4.4	10.7 12.7	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n High) S_{BA} or S_{AB} to $\overline{A}_n$ or $\overline{B}_n$	2	4.7 3.8	8.6 8.6	11.3 12.0	4.7 3.8	12.9 13.4	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n Low) S_{BA} or S_{AB} to $\overline{A}_n$ or $\overline{B}_n$	3	2.6 5.4	7.1 9.7	10.2 12.6	2.6 5.4	11.5 14.1	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to $\overline{A}_n$ or $\overline{B}_n$	5	4.2 4.3	9.2 9.8	13.0 13.9	4.2 4.3	14.6 15.6	ns
t_{PZH} t_{PZL}	Output Enable time DIR to $\overline{A}_n$ or $\overline{B}_n$	5	3.9 3.9	9.8 10.8	14.9 15.1	3.9 3.9	16.9 17.2	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to $\overline{A}_n$ or $\overline{B}_n$	5	5.7 5.3	8.7 8.1	11.3 10.5	5.7 5.3	12.2 11.4	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to $\overline{A}_n$ or $\overline{B}_n$	5	4.5 3.9	8.2 7.3	10.6 9.6	4.5 3.9	11.5 11.3	ns
t_s	Setup time (High or Low) $\overline{A}_n$ or $\overline{B}_n$ to CP_{AB} or CP_{BA}	4	5.0			5.0		ns
t_h	Hold time (High or Low) $\overline{A}_n$ or $\overline{B}_n$ to CP_{AB} or CP_{BA}	4	2.0			2.0		ns
t_w	Pulse width (High or Low) CP_{AB} or CP_{BA}	1	6.7			6.7		ns

AC WAVEFORMS

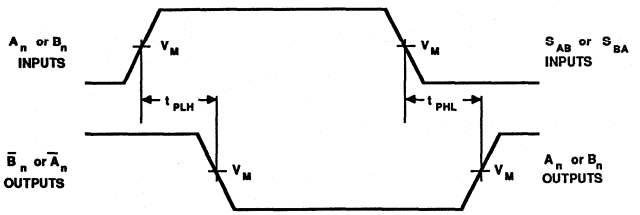


Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width

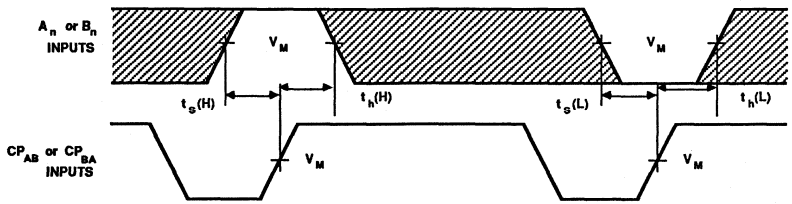


Waveform 2. Waveforms Showing Propagation Delay, S_{BA} or S_{AB} to A_n or B_n

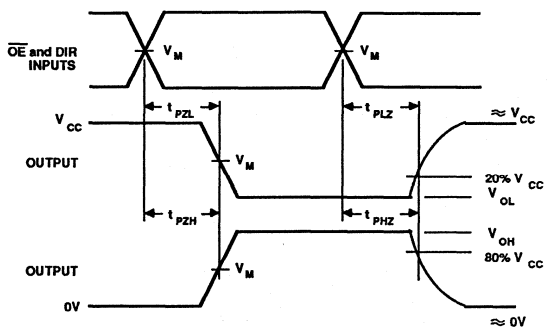
AC WAVEFORMS (Continued)



Waveform 3. Waveforms Showing Propagation Delay, A_n to B_n or B_n to A_n and S_{BA} or S_{AB} to A_n or B_n



Waveform 4. Waveforms Showing the Data Setup and Hold Times



Waveform 5. Waveforms Showing 3-State Output Enable and Disable Times

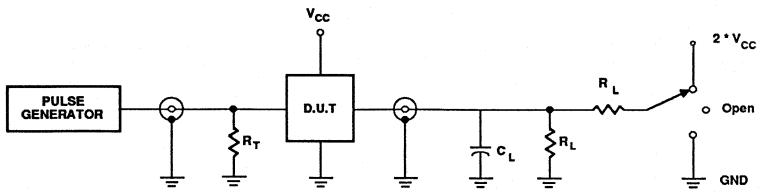
Octal transceiver/register with direction pin (3-State), INV

74AC/ACT11648

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11652

Octal transceiver/register with dual enable (3-State)

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11652 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11652 device is an octal transceiver/register featuring non-inverting 3-State bus compatible outputs in both send and receive directions, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data di-

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF		5.6	6.9	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled	60	59	pF
			Disabled	14	14	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{IO}	I/O capacitance	V_O = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency, CP_x to A or B	C_L = 50pF		125	125	MHz

Note:

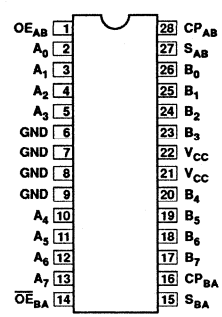
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

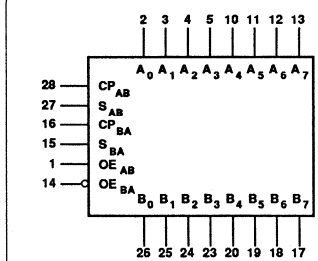
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11652N 74ACT11652N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11652D 74ACT11652D

PIN CONFIGURATION

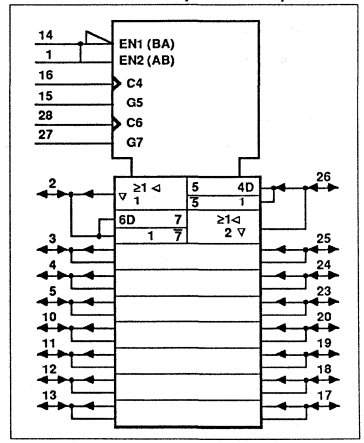
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver/register with dual enable (3-State)

74AC/ACT11652

rectly from the input bus or from internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a High logic level. Output Enable (OE_{AB}, $\overline{OE}_{BA}$) and Select pins (S_{AB}, S_{BA}) are provided for bus management. In the transceiver mode, data present at the High-impedance port may be stored in either the A or B register or both.

Figure 1 demonstrates the four fundamental bus-management functions that can be performed. The select pins (S_{AB}, S_{BA}) determine whether data is stored or transferred through the device in real-time. The Output Enable pins (OE_{AB}, $\overline{OE}_{BA}$) determine the direction of the data flow.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OE_{AB}	A-to-B output enable input
14	$\overline{OE}_{BA}$	B-to-A output enable input (active Low)
28	CP_{AB}	A-to-B clock input
16	CP_{BA}	B-to-A clock input
27	S_{AB}	A-to-B select input
15	S_{BA}	B-to-A select input
2, 3, 4, 5, 10, 11, 12, 13	A_0 - A_7	A side inputs/outputs (3-state)
26, 25, 24, 23, 20, 19, 18, 17	B_0 - B_7	B side inputs/outputs (3-state)
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

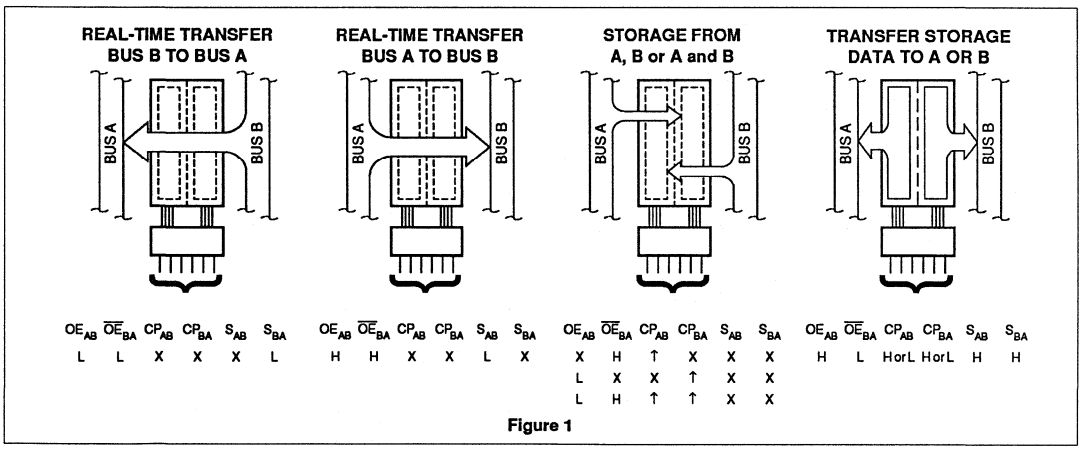


Figure 1

Octal transceiver/register with dual enable (3-State)

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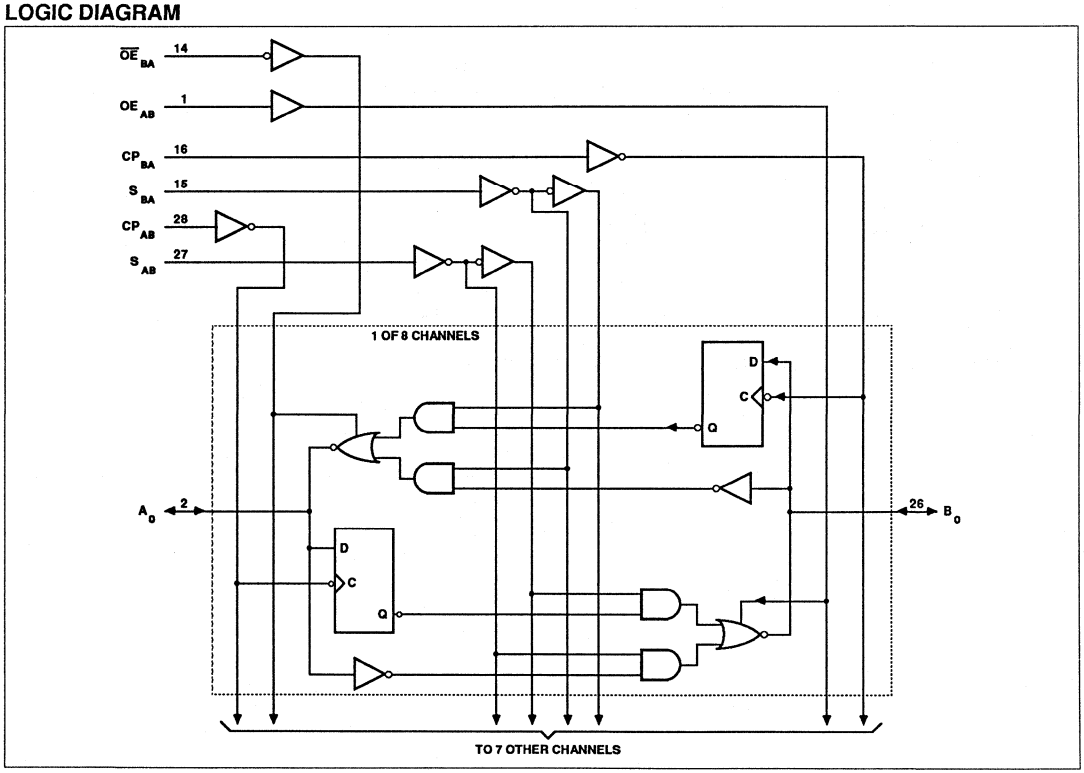
FUNCTION TABLE

OPERATING MODE	INPUTS						DATA I/O*	
	OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	$\overline{A}_0$ - $\overline{A}_7$	$\overline{B}_0$ - $\overline{B}_7$
Isolation Store A and B data	L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input
Store A, Hold B	X	H	↑	H or L	X	X	Input	unspecified*
Store A in both registers	H	H	↑	↑	L	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	unspecified*	Input
Store B in both registers	L	L	↑	↑	X	L	Output	Input
Real time B data to A bus Stored B data to A bus	L L	L L	X X	X H or L	X X	L H	Output	Input
Real time A data to B bus Stored A data to B bus	H H	H H	X H or L	X X	L H	X X	Input	Output
Stored A data to B bus Stored B data to A bus	H	L	H or L	H or L	H	H	Output	Output

* The data output functions may be enabled or disabled by various signals at the OE_{AB} and the $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

un = unspecified
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



Octal transceiver/register with dual enable (3-State)

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11652			74ACT11652			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±400	mA
	DC ground current		±400	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal transceiver/register with dual enable (3-State)

74AC/ACT11652

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11652				74ACT11652				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off–state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11652					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	65	80		65		MHz
t_{PLH} t_{PHL}	Propagation delay CP_{AB} or CP_{BA} to A_n or B_n	1	4.3 5.3	11.2 13.1	14.3 16.2	4.3 5.3	16.2 17.8	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	3	2.9 3.9	8.5 10.3	11.1 12.9	2.9 3.9	12.9 14.2	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n High) S_{BA} or S_{AB} to A_n or B_n	2	3.4 4.7	9.4 11.5	12.0 14.3	3.4 4.7	13.7 15.6	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n Low) S_{BA} or S_{AB} to A_n or B_n	3	3.9 4.8	10.5 12.1	13.3 16.3	3.9 4.8	14.9 17.7	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_{BA}$ to A_n	5	4.3 5.2	11.1 14.4	14.5 19.8	4.3 5.2	16.5 22.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n	5	3.7 3.5	6.4 6.0	8.1 7.8	3.7 3.5	8.5 8.2	ns
t_{PZH} t_{PZL}	Output Enable time OE_{AB} to B_n	5	4.7 5.6	11.6 14.8	15.0 19.9	4.7 5.6	16.9 21.9	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to B_n	5	4.0 3.5	6.6 6.1	8.2 7.7	4.0 3.5	8.6 8.0	ns
t_s	Setup time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	6.0			6.0		ns
t_h	Hold time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	1.0			1.0		ns
t_w	Pulse width (High or Low) CP_{AB} or CP_{BA}	1	7.7			7.7		ns

Octal transceiver/register with dual enable (3-State)

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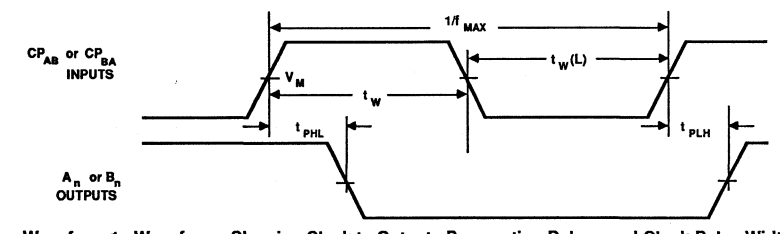
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11652					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_{AB} or CP_{BA} to A_n or B_n	1	3.6 4.4	6.7 7.8	9.5 10.8	3.6 4.4	10.7 12.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	3	2.4 3.1	5.2 6.0	7.6 8.7	2.4 3.1	8.6 9.6	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n High) S_{BA} or S_{AB} to A_n or B_n	2	2.9 3.8	5.6 6.9	8.1 9.6	2.9 3.8	9.1 10.7	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n Low) S_{BA} or S_{AB} to A_n or B_n	3	3.3 4.0	6.2 7.1	8.8 9.9	3.3 4.0	9.9 10.9	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_{BA}$ to A_n	5	3.3 4.2	6.6 7.4	9.6 10.9	3.3 4.2	10.9 12.2	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n	5	3.6 3.3	5.5 5.0	7.2 6.7	3.6 3.3	7.6 7.1	ns
t_{PZH} t_{PZL}	Output Enable time OE_{AB} to B_n	5	4.1 4.6	7.2 7.9	10.1 11.1	4.1 4.6	11.3 12.3	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to B_n	5	3.9 3.4	5.6 5.2	7.3 6.8	3.9 3.4	7.6 7.2	ns
t_s	Setup time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	4.5			4.5		ns
t_h	Hold time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	1.0			1.0		ns
t_w	Pulse width (High or Low) CP_{AB} or CP_{BA}	1	5.0			5.0		ns

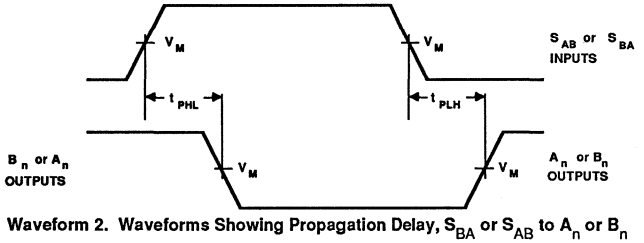
AC ELECTRICAL CHARACTERISTICS AT 5.5V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11652					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP_{AB} or CP_{BA} to A_n or B_n	1	5.4 6.1	8.4 9.4	11.8 13.1	5.4 6.1	13.1 14.4	ns
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to B_n or A_n	3	3.8 3.4	7.0 6.7	9.9 10.7	3.8 3.4	11.1 11.6	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n High) S_{BA} or S_{AB} to A_n or B_n	2	2.8 5.5	6.2 8.7	10.1 12.1	2.8 5.5	11.0 13.3	ns
t_{PLH} t_{PHL}	Propagation delay (A_n or B_n Low) S_{BA} or S_{AB} to A_n or B_n	3	4.9 3.9	7.8 7.5	11.0 11.6	4.9 3.9	12.2 12.6	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}_{BA}$ to A_n	5	3.3 4.1	7.2 7.8	11.4 12.6	3.3 4.1	12.6 13.8	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}_{BA}$ to A_n	5	5.2 4.8	7.2 6.7	9.3 8.6	5.2 4.8	9.9 9.3	ns
t_{PZH} t_{PZL}	Output Enable time OE_{AB} to B_n	5	5.1 5.8	9.1 9.7	13.4 14.2	5.1 5.8	15.2 16.1	ns
t_{PHZ} t_{PLZ}	Output disable time OE_{AB} to B_n	5	3.4 3.1	6.8 6.0	9.7 8.8	3.4 3.1	10.3 9.3	ns
t_s	Setup time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	4.0			4.0		ns
t_h	Hold time (High or Low) A_n or B_n to CP_{AB} or CP_{BA}	4	2.5			2.5		ns
t_w	Pulse width (High or Low) CP_{AB} or CP_{BA}	1	5.0			5.0		ns

AC WAVEFORMS

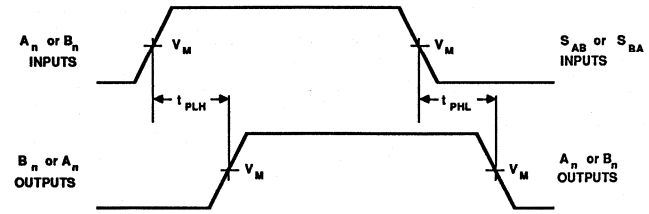


Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width

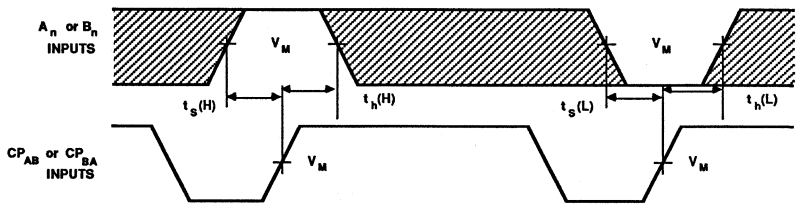


Waveform 2. Waveforms Showing Propagation Delay, S_{BA} or S_{AB} to A_n or B_n

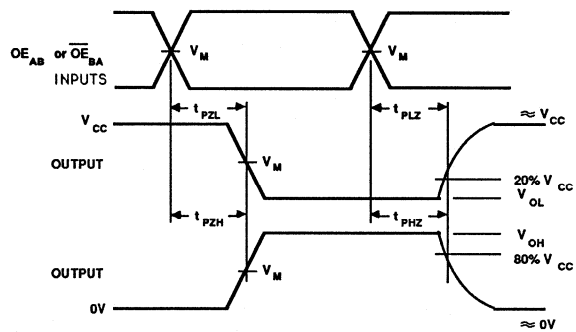
AC WAVEFORMS (Continued)



Waveform 3. Waveforms Showing Propagation Delay, A_n to B_n or B_n to A_n and S_{BA} or S_{AB} to A_n or B_n



Waveform 4. Waveforms Showing the Data Setup and Hold Times

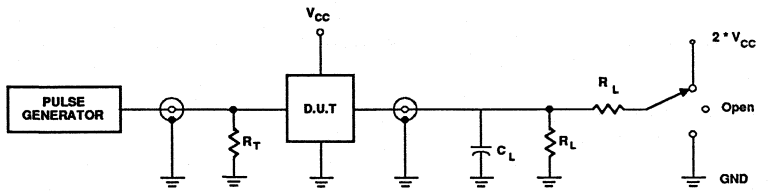


Waveform 5. Waveforms Showing 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	August 13, 1990
Status	Preliminary Specification
ACL Products	

AC11657: Objective Specification
ACT11657: Preliminary Specification
Octal transceiver with 8-bit parity checker/generator

FEATURES

- 3-State outputs
- Combines '245 and '280 functions in one package
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11657 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11657 device is an octal transceiver featuring non-inverting buffers and an 8-bit parity generator/checker, and is intended for bus-oriented applications.

The Transmit/Receive ($T/\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active-High) enables data

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to B_n	C_L = 50pF			5.3	ns
C_{PD}	Power dissipation capacitance per transceiver[1]	f = 1MHz; C_L = 50pF	Enabled		95	pF
			Disabled		21	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		10	10	pF
C_{IO}	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

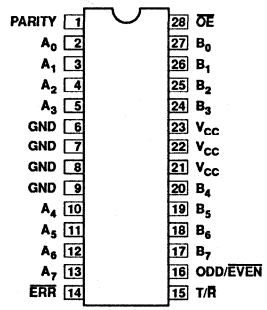
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

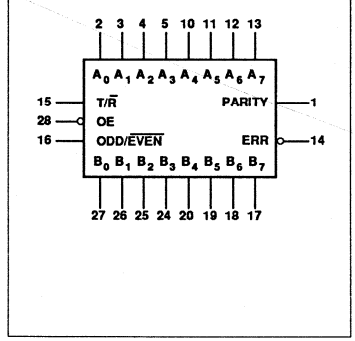
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11657N 74ACT11657N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11657D 74ACT11657D

PIN CONFIGURATION

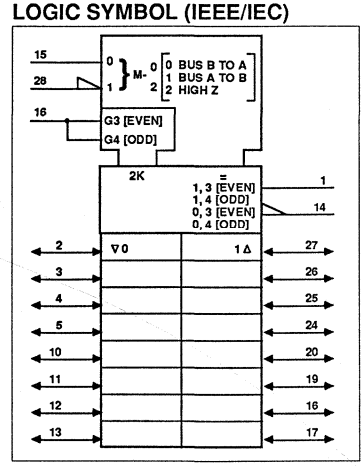
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver with 8-bit parity checker/generator

74AC/ACT11657

from A ports to B ports; Receive (active-Low) enables data from B ports to A ports.

The Output Enable ($\overline{OE}$) input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is High. The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems. The parity (PARITY) pin is an output from the generator/checker when transmitting from port A to B (T/$\overline{R}$ = High) and an input when receiving from port B to A (T/$\overline{R}$ = Low). When transmitting (T/$\overline{R}$ = High) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{EVEN}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode (T/$\overline{R}$ = Low) the B port is polled to determine the number of High bits.

If parity select (ODD/$\overline{EVEN}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{ERR}$ will be High, signifying no error.

(2) even and the parity (PARITY) input is High, then $\overline{ERR}$ will be asserted Low, indicating an error.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
15	T/$\overline{R}$	Transmit/receive input
16	ODD/$\overline{EVEN}$	Parity select input
28	$\overline{OE}$	Output enable input (active-Low)
2, 3, 4, 5, 10, 11, 12, 13	A_0 - A_7	A ports 3-State inputs/output
27, 26, 25, 24, 20, 19, 18, 17	B_0 - B_7	B ports 3-State inputs/output
1	PARITY	Parity input/output
14	$\overline{ERR}$	Error output
6, 7, 8, 9	GND	Ground (0V)
21, 22, 23	V_{CC}	Positive supply voltage

FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/ OUTPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1,3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

Octal transceiver with 8-bit parity checker/generator

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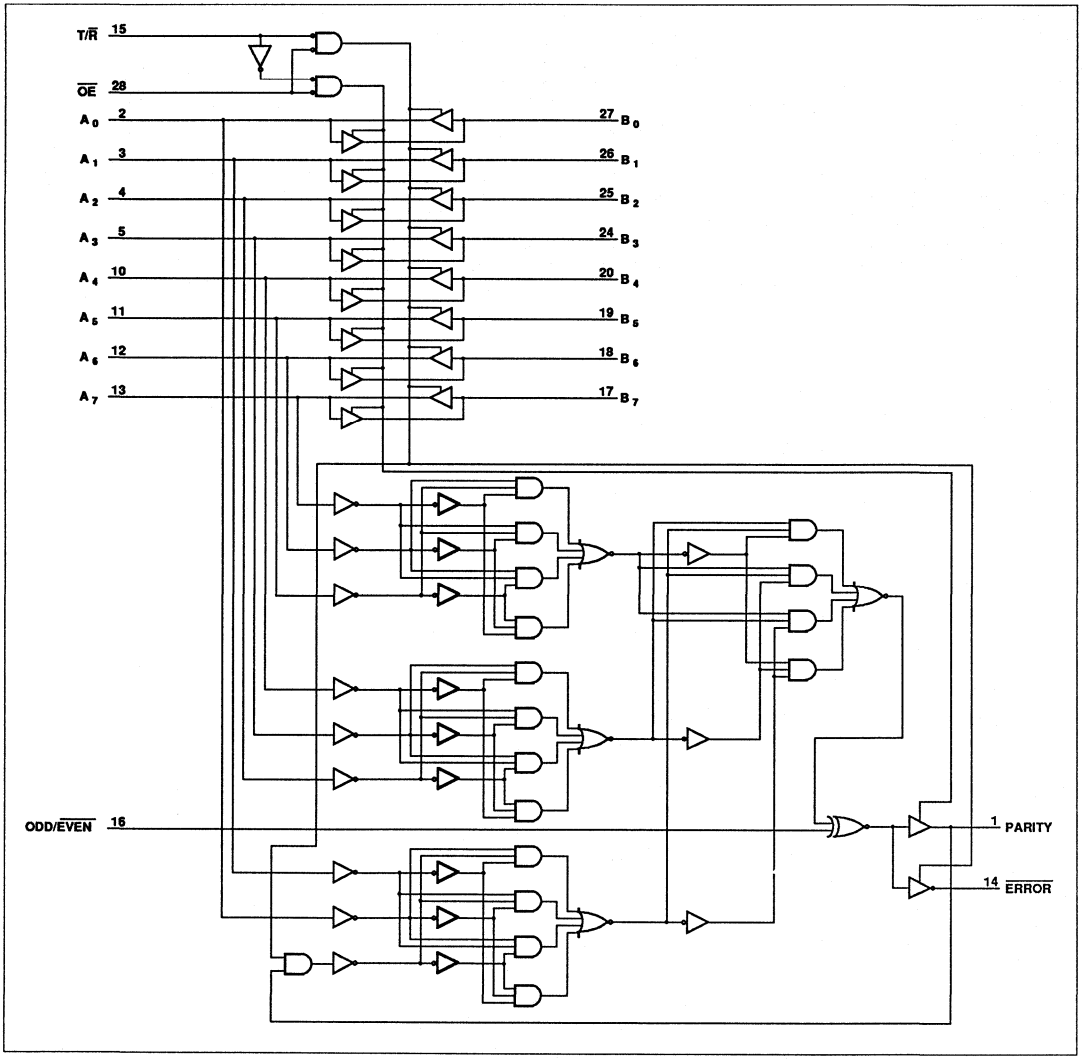
LOGIC DIAGRAM



Octal transceiver with 8-bit parity checker/generator

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		74AC11657			74ACT11657			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage		3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	$\overline{OE}$ only	0		10	0		10	ns/V
		All other inputs	0		5	0		5	
T_{amb}	Operating free-air temperature range		-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11657				74ACT11657				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Octal transceiver with 8-bit parity checker/generator

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AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11657					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay, A_n to B_n or B_n to A_n	1						ns
t_{PLH} t_{PHL}	Propagation delay, A_n to PARITY	1						ns
t_{PLH} t_{PHL}	Propagation delay, ODD/$\overline{EVEN}$ to $\overline{PARITY}$, $\overline{ERROR}$	1						ns
t_{PLH} t_{PHL}	Propagation delay, B_n to $\overline{ERROR}$	1						ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{PARITY}$ to $\overline{ERROR}$	1						ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2						ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2						ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11657					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay, A_n to B_n or B_n to A_n	1						ns
t_{PLH} t_{PHL}	Propagation delay, A_n to PARITY	1						ns
t_{PLH} t_{PHL}	Propagation delay, ODD/$\overline{EVEN}$ to $\overline{PARITY}$, $\overline{ERROR}$	1						ns
t_{PLH} t_{PHL}	Propagation delay, B_n to $\overline{ERROR}$	1						ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{PARITY}$ to $\overline{ERROR}$	1						ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2						ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2						ns

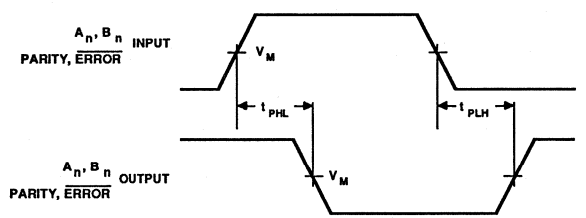
Octal transceiver with 8-bit parity checker/generator

74AC/ACT11657

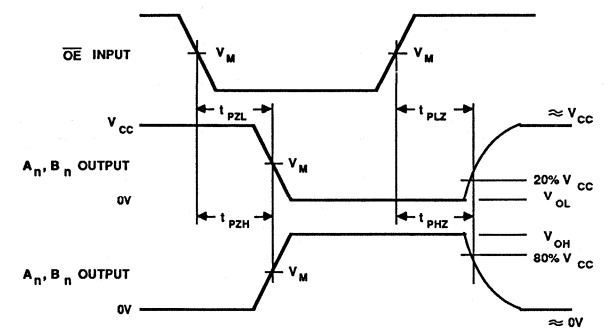
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11657					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay, A_n to B_n or B_n to A_n	1	3.2 2.2	5.5 5.1	6.9 7.2	3.2 2.2	7.6 7.8	ns
t_{PLH} t_{PHL}	Propagation delay, A_n to PARITY	1	3.6 4.0	7.5 8.1	10.3 10.7	3.6 4.0	11.5 12.0	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{ODD/EVEN}$ to $\overline{PARITY}$, $\overline{ERROR}$	1	2.8 3.1	6.0 6.4	7.8 8.3	2.8 3.1	8.7 9.1	ns
t_{PLH} t_{PHL}	Propagation delay, B_n to $\overline{ERROR}$	1	4.6 4.9	12.4 12.8	16.9 17.7	4.6 4.9	19.4 20.2	ns
t_{PLH} t_{PHL}	Propagation delay, $\overline{PARITY}$ to $\overline{ERROR}$	1	4.1 3.9	7.7 7.7	10.0 10.4	4.1 3.9	11.1 11.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	3.2 3.9	6.2 7.5	9.8 10.5	3.2 3.9	10.5 11.6	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	4.5 4.8	7.5 7.4	10.1 9.3	4.5 4.8	10.9 10.0	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (A_n, B_n) to Output (B_n, A_n) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

Octal transceiver with 8-bit parity checker/generator

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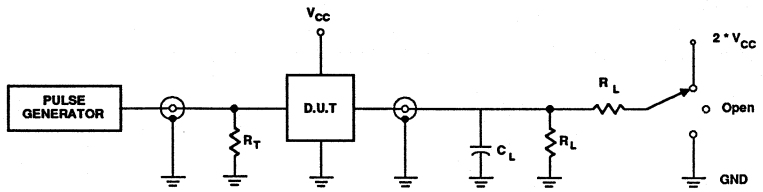
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11810

Quad 2-input Exclusive-NOR gate

FEATURES

- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: SSI

DESCRIPTION

The 74AC/ACT11810 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11810 provides four separate 2-input exclusive-NOR gate functions.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay A, B, to $\overline{Y}$	C_L = 50pF	3.9	4.9	ns
C_{PD}	Power dissipation capacitance per gate[1]	f = 1MHz; C_L = 50pF	24	26	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

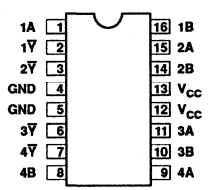
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

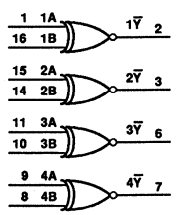
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11810N 74ACT11810N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11810D 74ACT11810D

PIN CONFIGURATION

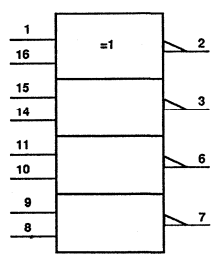
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Quad 2-input Exclusive-NOR gate | 74AC/ACT11810

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 15, 11, 9	1A - 4A	Data inputs
16, 14, 10, 8	1B - 4B	Data inputs
2, 3, 6, 7	$1\overline{Y}$ - $4\overline{Y}$	Data outputs
4, 5	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	$n\overline{Y}$
L	L	H
L	H	L
H	L	L
H	H	H

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11810			74ACT11810			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±100	mA
	DC ground current		±100	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11810				74ACT11810				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		4.0		40		4.0		40	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11810					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.7 1.8	5.5 5.1	7.7 7.0	1.7 1.8	9.0 8.3	ns

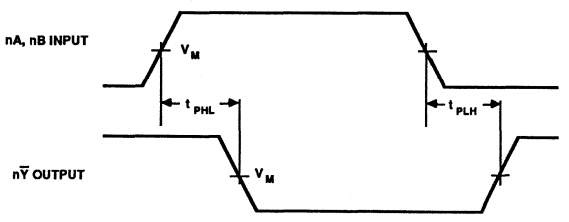
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11810					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.5 1.6	3.9 3.9	6.1 5.8	1.5 1.6	7.0 7.0	ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11810					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA, nB to n$\overline{Y}$	1	1.9 1.9	4.8 4.9	7.2 7.1	1.9 1.9	8.3 8.3	ns

AC WAVEFORMS

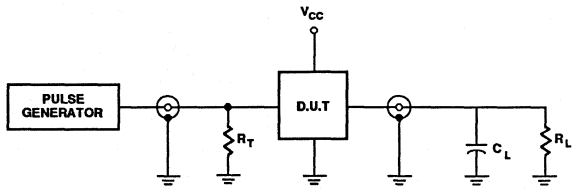


Waveform 1. Waveforms Showing the Input (nA, nB) to Output (n$\overline{Y}$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11827

10-wide buffer/line driver (3-State)

FEATURES

- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11827 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11827 device is a 10-wide buffer/line driver and provides high performance bus interface buffering for wide data/address paths or busses carrying parity. It has NOR Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) for maximum control flexibility.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to Y_n	C_L = 50pF		5.8	6.6	ns
C_{PD}	Power dissipation capacitance per buffer[1]	f = 1MHz; C_L = 50pF	Enabled	35	35	pF
			Disabled	9	10	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

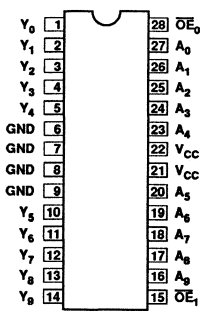
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_o = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

ORDERING INFORMATION

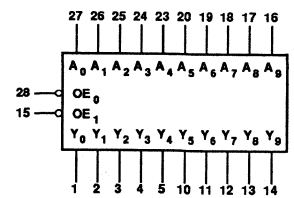
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11827N 74ACT11827N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11827D 74ACT11827D

PIN CONFIGURATION

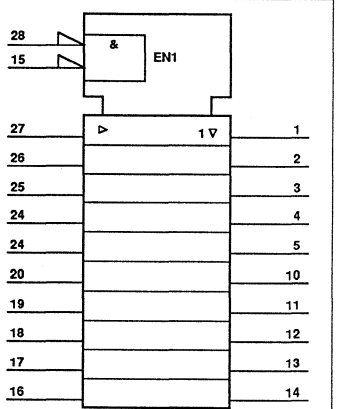
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



10-wide buffer/line driver (3-State) 74AC/ACT11827

PIN DESCRIPTION

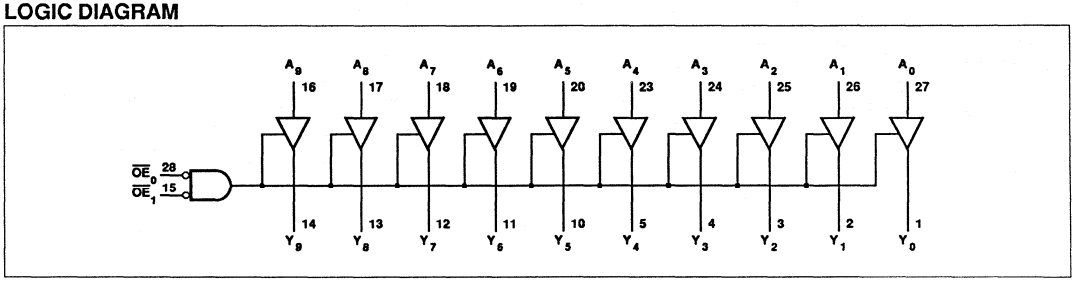
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28, 15	$\overline{OE}_0$, $\overline{OE}_1$	Output enable input (active Low)
27, 26, 25, 24, 23, 20, 19, 18, 17, 16	A_0 - A_9	Data inputs
1, 2, 3, 4, 5, 10, 11, 12, 13, 14	Y_0 - Y_9	Data inputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}_n$	A_n	Y_n
L	L	L
L	H	H
H	X	Z

H = Highvoltage level
L = Low voltage level
X = Don't care
Z = High-impedance

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11827			74ACT11827			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

10-wide buffer/line driver (3-State) 74AC/ACT11827

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11827				74ACT11827				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off–state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

10-wide buffer/line driver (3-State) 74AC/ACT11827

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11827					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	4.8 6.8	8.4 10.4	10.8 12.6	4.8 6.8	12.4 13.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	6.3 10.0	10.2 16.0	12.7 19.2	6.3 10.0	14.5 21.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	5.9 5.4	8.5 8.0	10.4 10.0	5.9 5.4	11.1 10.5	ns

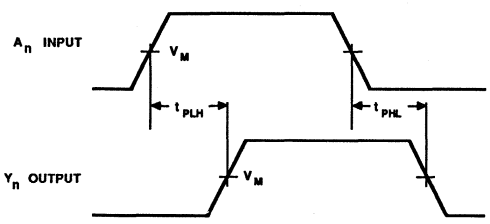
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11827					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	2.1 2.9	5.3 6.2	7.5 8.4	2.1 2.9	8.7 9.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	3.1 4.1	5.9 7.7	8.2 10.6	3.1 4.1	9.7 13.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	3.9 4.0	6.6 6.3	8.4 7.9	3.9 4.0	9.1 8.8	ns

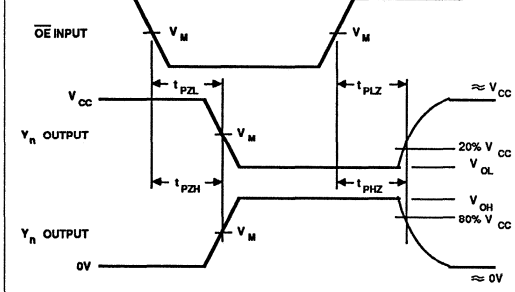
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11827					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	3.8 2.7	6.3 6.9	8.0 9.5	3.8 2.7	9.2 11.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	2.6 3.2	6.4 8.0	9.2 11.2	2.6 3.2	11.3 14.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	6.1 5.8	8.8 8.3	11.1 10.6	6.1 5.8	12.0 11.6	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (A_n) to Output (Y_n) Propagation Delays



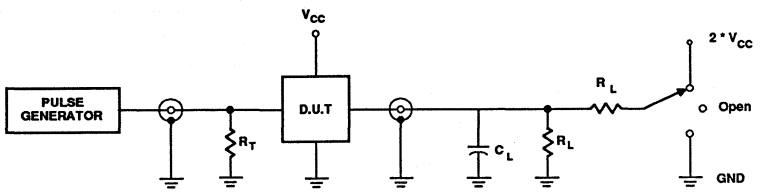
Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

10-wide buffer/line driver (3-State) 74AC/ACT11827

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	February 19, 1990
Status	Preliminary Specification
ACL Products	

74AC/ACT11828

10-wide buffer/line driver (3-State), INV

FEATURES

- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11828 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11828 device is a 10-wide buffer/line driver and provides high performance bus interface buffering for wide data/address paths or busses carrying parity. It has NOR Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) for maximum control flexibility.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	C_L = 50pF		5.7	6.8	ns
C_{PD}	Power dissipation capacitance per buffer[1]	f = 1MHz; C_L = 50pF	Enabled	37	37	pF
			Disabled	11	11	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC}; Disabled		12	12	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

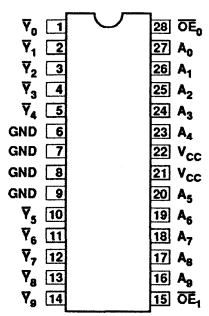
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

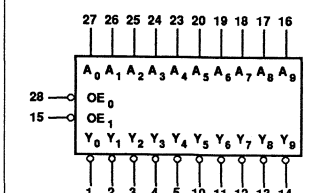
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11828N 74ACT11828N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11828D 74ACT11828D

PIN CONFIGURATION

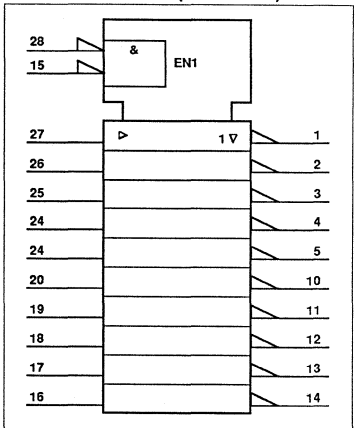
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



10-wide buffer/line driver (3-State), INV | 74AC/ACT11828

PIN DESCRIPTION

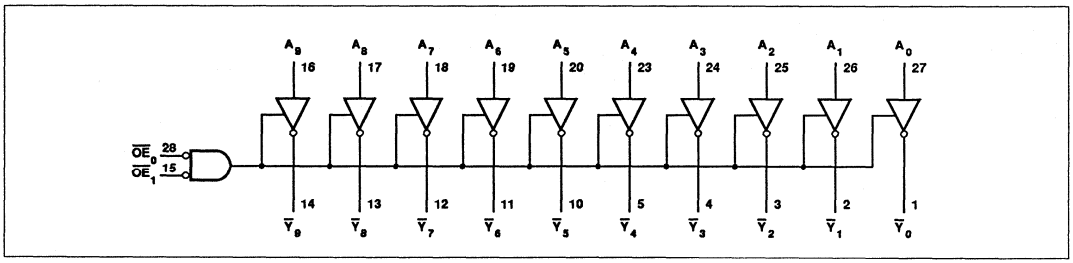
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28, 15	$\overline{OE}_0$, $\overline{OE}_1$	Output enable input (active Low)
27, 26, 25, 24, 23, 20, 19, 18, 17, 16	A_0 - A_9	Data inputs
1, 2, 3, 4, 5, 10, 11, 12, 13, 14	$\overline{Y}_0$ - $\overline{Y}_9$	Data inputs
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}_n$	A_n	$\overline{Y}_n$
L	L	H
L	H	L
H	X	Z

H = Highvoltage level
L = Low voltage level
X = Don't care
Z = High-impedance

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11828			74ACT11828			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

10-wide buffer/line driver (3-State), INV 74AC/ACT11828

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11828				74ACT11828				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

10-wide buffer/line driver (3-State), INV — 74AC/ACT11828

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11828					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	5.4 7.2	9.8 10.4	12.7 13.2	5.4 7.2	14.3 14.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	6.5 9.5	10.8 15.0	14.4 19.2	6.5 9.5	16.3 21.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	5.3 5.1	8.2 7.9	11.0 10.5	5.3 5.1	11.9 11.2	ns

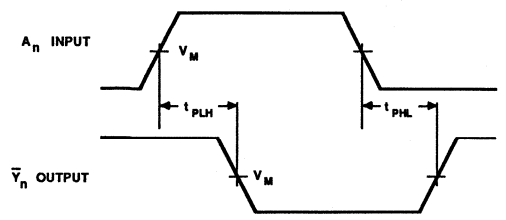
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11828					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	2.4 3.2	5.2 6.2	7.9 8.9	2.4 3.2	9.5 10.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	3.1 3.8	6.4 7.7	8.8 10.5	3.1 3.8	10.7 13.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	3.7 3.9	6.4 6.2	8.8 8.2	3.7 3.9	9.6 9.2	ns

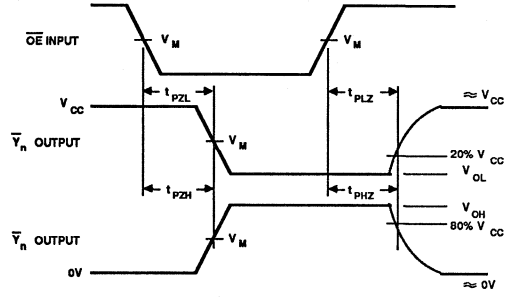
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11828					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.9 5.2	5.6 8.0	8.3 10.3	1.9 5.2	10.2 11.7	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	2.9 3.4	7.0 8.3	9.9 11.4	2.9 3.4	12.1 14.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	6.0 5.9	9.0 8.5	11.3 10.9	6.0 5.9	12.3 11.7	ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Input (A_n) to Output ($\overline{Y}_n$) Propagation Delays

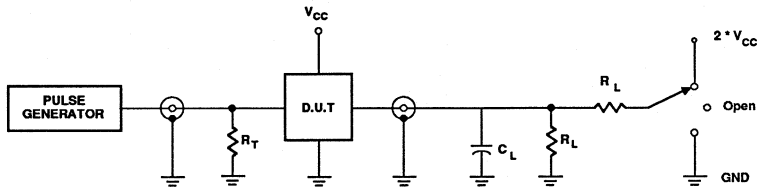


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Preliminary Specification
ACL Products	

74AC/ACT11873

Dual 4-bit D-type transparent latch with clear (3–State)

FEATURES

- 3-State output buffers
- Asynchronous clear
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11873 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11873 devices are dual 4-bit D-type latches with asynchronous resets, making them suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit latches are transparent D-type. When the latch enable inputs (1LE, 2LE) are High, the data on the D

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay nD_n to nQ_n	C_L = 50pF		5.5	6.9	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	Enabled	43	40	pF
			Disabled	9	7	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		13.5	13.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA

Note:

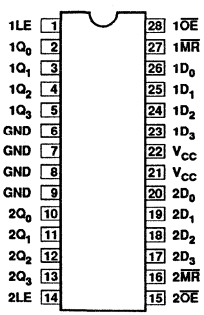
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

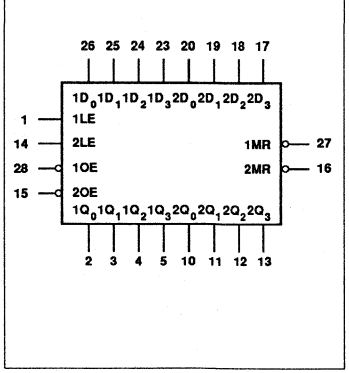
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11873N 74ACT11873N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11873D 74ACT11873D

PIN CONFIGURATION

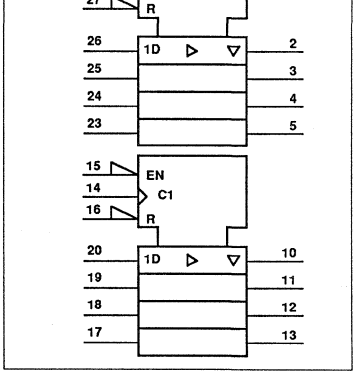
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Dual 4-bit D-type transparent latch with clear (3–State)

74AC/ACT11873

inputs is transferreded to the latch outputs (Q_0 - Q_3). The latches remain transparent to the data input while LE is High and store the data that is present one setup time before the High-to-Low latch enable transition. All four Q outputs will be forced low, independent of clock or data inputs, by taking $\overline{MR}$ Low.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When the $\overline{OE}$ inputs are Low, the latched or transparent data appears at the outputs. When the $\overline{OE}$ inputs are high, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

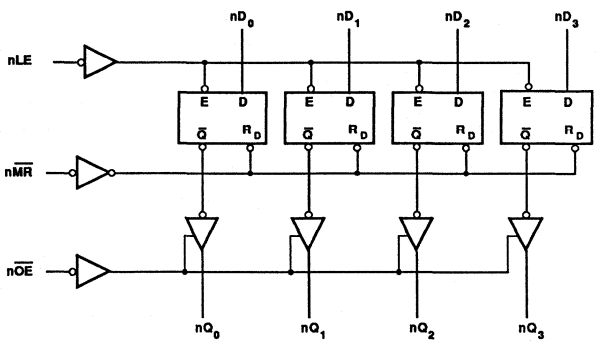
PIN NUMBER	SYMBOL	NAME AND FUNCTION
28, 15	$1\overline{OE}$, $2\overline{OE}$	Output enables
26, 25, 24, 23, 20, 19, 18, 17	$1D_0$ - $1D_3$, $2D_0$ - $2D_3$	Data inputs
2, 3, 4, 5 10, 11, 12, 13	$1Q_0$ - $1Q_3$, $2Q_0$ - $2Q_3$	Data outputs
1, 14	1LE, 2LE	Latch enable inputs
27, 16	$1\overline{MR}$, $2\overline{MR}$	Master reset inputs
6, 7, 8, 9	GND	Ground (0V)
22, 21	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS				INTERNAL REGISTER	OUTPUTS
	$\overline{MR}$	$n\overline{OE}$	nLE	nD_n		nQ_n
Reset (clear)	L	L	X	X	X	L
Enable and read register	H H	L L	H H	L H	L H	L H
Latch and read register	H H	L L	↓ ↓	l h	L H	L H
Hold	H	L	L	X	NC	NC
Disable outputs	X	H	X	X	X	Z

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
NC = No change
Z = High-impedance "OFF" state
↓= Low-to-High transition

LOGIC DIAGRAM



Dual 4-bit D-type transparent latch with clear (3–State)

74AC/ACT11873

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11873			74ACT11873			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Dual 4-bit D-type transparent latch with clear (3–State)

74AC/ACT11873

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11873				74ACT11873				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off–state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Dual 4-bit D-type transparent latch with clear (3–State)

74AC/ACT11873

AC ELECTRICAL CHARACTERISTICS AT 3.0V ±0.3V

SYMBOL	PARAMETER		WAVEFORM	74AC11873					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nD_n to nQ_n		1	2.8 2.8	8.8 9.0	11.2 11.2	2.8 2.8	13.0 12.7	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQ_n		5	3.0 2.9	9.4 9.4	11.8 11.7	3.0 2.9	13.6 13.2	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n		4	2.3	8.2	10.3	2.3	11.5	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		2	1.8 2.7	6.4 9.9	8.4 12.5	1.8 2.7	9.7 14.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		2	3.8 3.5	6.8 6.8	8.4 8.5	3.8 3.5	9.0 9.1	ns
t_W	nLE pulse width High or Low		5	5.0			5.0		ns
t_W	$n\overline{MR}$ pulse width Low		4	5.0			5.0		ns
t_S	Setup time nD_n to nLE	Data High	3	3.0			3.0		ns
		Data Low		4.0			4.0		
t_H	Hold time nD_n to nLE	Data High	3	1.0			1.0		ns
		Data Low		1.0			1.0		

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74AC11873					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nD_n to nQ_n		1	2.2 2.1	5.5 5.5	7.3 7.2	2.2 2.1	8.4 8.2	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQ_n		5	2.4 2.2	5.9 5.8	7.8 7.6	2.4 2.2	8.9 8.7	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n		4	1.7	5.1	6.8	1.7	7.6	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		2	1.2 1.9	4.1 5.5	5.6 7.3	1.2 1.9	6.4 8.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		2	3.5 3.3	5.9 5.5	7.4 7.0	3.5 3.3	7.9 7.6	ns
t_W	nLE pulse width High or Low		5	5.0			5.0		ns
t_W	$n\overline{MR}$ pulse width Low		4	5.0			5.0		ns
t_S	Setup time nD_n to nLE	Data High	3	2.0			2.0		ns
		Data Low		3.0			3.0		
t_H	Hold time nD_n to nLE	Data High	3	1.0			1.0		ns
		Data Low		1.0			1.0		

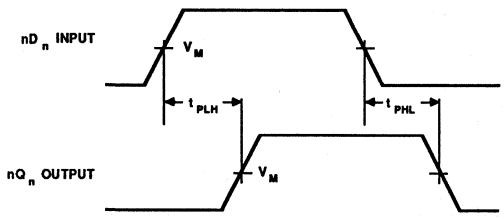
Dual 4-bit D-type transparent latch with clear (3–State)

74AC/ACT11873

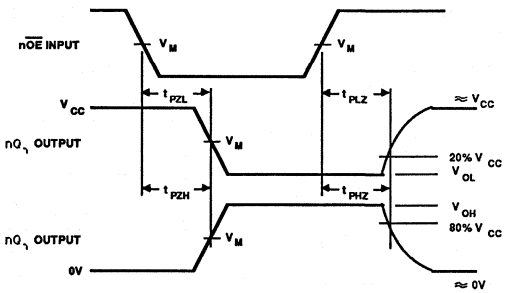
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER		WAVEFORM	74ACT11873					UNIT
				T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nD_n to nQ_n		1	4.4 3.0	7.2 6.6	8.8 9.1	4.4 3.0	10.0 10.2	ns
t_{PLH} t_{PHL}	Propagation delay nLE to nQ_n		5	4.7 5.2	8.1 8.9	10.0 10.9	4.7 5.2	11.3 12.3	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n		4	2.9	6.5	9.0	2.9	10.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level		2	1.9 2.7	4.9 6.4	7.1 9.1	1.9 2.7	8.0 10.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level		2	5.7 5.2	8.0 7.8	9.5 9.1	5.7 5.2	10.2 9.8	ns
t_W	nLE pulse width High or Low		5	5.0			5.0		ns
t_W	$n\overline{MR}$ pulse width Low		4	5.0			5.0		ns
t_S	Setup time nD_n to nLE	Data High	3	6.0			6.0		ns
		Data Low		3.0			3.0		
t_H	Hold time nD_n to nLE	Data High	3	0.0			0.0		ns
		Data Low		0.0			0.0		

AC WAVEFORMS

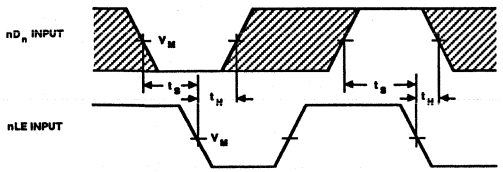


Waveform 1. Waveforms Showing the Input (nD_n) to Output (nQ_n) Propagation Delays

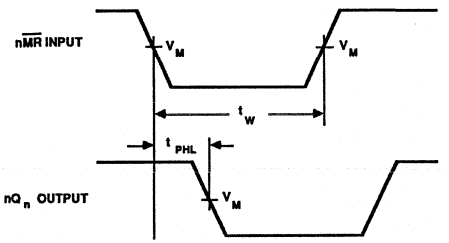


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

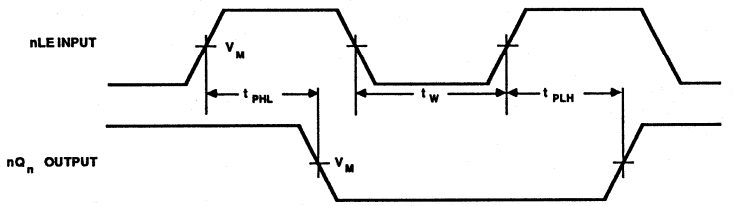
WAVEFORMS (continued)



Waveform 3. Waveforms Showing the Data Setup and Hold Times for nD$_n$ Input to nLE Input



Waveform 4. Waveforms Showing Master Reset (nMR) Pulse Width and Master Reset to Output Delay

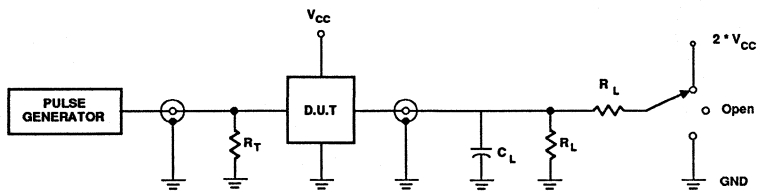


Waveform 5. Waveforms Showing the Latch Enable Input (nLE) Pulse Width and the Latch Enable Input to Output (nQ$_n$) Propagation Delays

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Preliminary Specification
ACL Products	

74AC/ACT11874

Dual 4-bit D-type edge-triggered flip-flop with clear (3–State)

FEATURES

- 3-State output buffers
- Asynchronous clear
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11874 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11874 devices are dual 4-bit D-type edge-triggered flip-flops with asynchronous resets, making them suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The edge-triggered flip-flops enter data on the low-to-high transition of the clock. All four Q outputs will be forced low, in-

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V		TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/t_{PHL}	Propagation delay nCP to Q_n	C_L = 50pF		5.6	7.2	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz;	Enabled	31	35	pF
		C_L = 50pF	Disabled	13	17	
C_{IN}	Input capacitance	V_I = 0V or V_{CC}		4.5	4.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}; Disabled		13.5	13.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17		500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF; V_{CC} = 5.5V		140	140	MHz

Note:

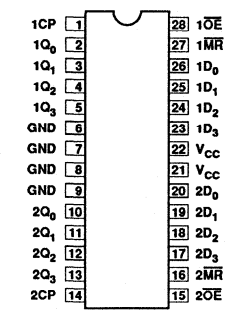
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

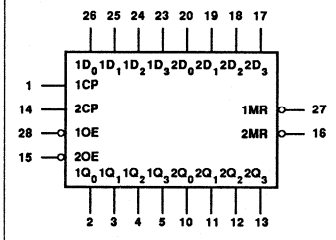
PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11874N 74ACT11874N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11874D 74ACT11874D

PIN CONFIGURATION

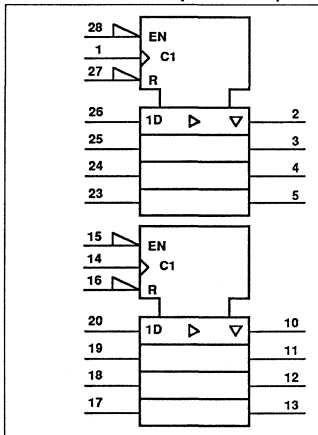
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Dual 4-bit D-type edge-triggered flip-flop with clear (3–State)

74AC/ACT11874

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
28, 15	$1\overline{OE}$, $2\overline{OE}$	Output enables
26, 25, 24, 23, 20, 19, 18, 17	$1D_0$ - $1D_3$, $2D_0$ - $2D_3$	Data inputs
2, 3, 4, 5, 10, 11, 12, 13	$1Q_0$ - $1Q_3$, $2Q_0$ - $2Q_3$	Data outputs
1, 14	1CP, 2CP	Clock inputs
27, 16	$1\overline{MR}$, $2\overline{MR}$	Master reset inputs
6, 7, 8, 9	GND	Ground (0V)
22, 21	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS
	$\overline{MR}$	$n\overline{OE}$	nCP	nD_n	nQ_n
Reset (clear)	L	L	X	X	L
Load flip-flop	H H	L L	↑ ↑	l h	L H
Disable outputs	X	H	X	X	Z

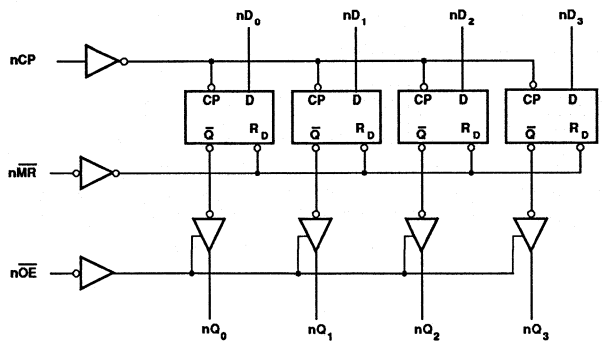
H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
Z = High-impedance "OFF" state
↑ = Low-to-High transition

dependent of clock or data inputs, by taking $\overline{MR}$ Low.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable (OE) controls all eight 3-State buffers independent of the latch operation.

When the $\overline{OE}$ inputs are Low, the latched or transparent data appears at the outputs. When the $\overline{OE}$ inputs are high, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM



Dual 4-bit D-type edge-triggered flip-flop with clear (3–State)

74AC/ACT11874

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11874			74ACT11874			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Dual 4-bit D-type edge-triggered flip-flop with clear (3–State)

74AC/ACT11874

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11874				74ACT11874				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	$V_I = V_{IL}$ or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	$V_I = V_{CC}$ or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off–state current	$V_I = V_{IL}$ or V_{IH}, $V_O = V_{CC}$ or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	$V_I = V_{CC}$ or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Dual 4-bit D-type edge-triggered flip-flop with clear (3–State)

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AC ELECTRICAL CHARACTERISTICS AT 3.0V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11874					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	60	80		60		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQ_n	1	2.9 3.7	7.3 8.8	11.0 13.1	2.9 3.7	12.5 14.6	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n	4	3.9	9.3	14.0	3.9	15.7	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	2	2.1 3.1	5.6 8.4	8.7 13.1	2.1 3.1	9.8 14.9	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	2	4.0 3.9	6.2 6.3	8.2 8.5	4.0 3.9	8.7 9.0	ns
t_W	Clock pulse width High or Low	1	8.3			8.3		ns
t_W	$n\overline{MR}$ pulse width Low	4	4.0			4.0		ns
t_S	Setup time nD_n to nCP	3	3.0			3.0		ns
t_H	Hold time nD_n to nCP	3	1.0			1.0		ns
t_{rec}	Recovery time $n\overline{MR}$ to nCP	4	1.5			1.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11874					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	140		125		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQ_n	1	2.3 2.9	5.2 6.1	7.4 8.6	2.3 2.9	8.3 9.6	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n	4	2.9	6.3	8.9	2.9	10.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	2	1.5 2.3	4.0 5.4	5.9 7.8	1.5 2.3	6.6 8.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	2	3.8 3.7	5.7 5.5	7.3 7.1	3.8 3.7	7.7 7.5	ns
t_W	Clock pulse width High or Low	1	4.0			4.0		ns
t_W	$n\overline{MR}$ pulse width Low	4	4.0			4.0		ns
t_S	Setup time nD_n to nCP	3	2.0			2.0		ns
t_H	Hold time nD_n to nCP	3	1.0			1.0		ns
t_{rec}	Recovery time $n\overline{MR}$ to nCP	4	1.5			1.5		ns

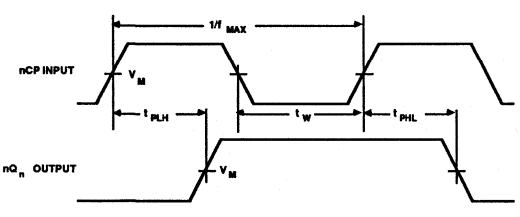
Dual 4-bit D-type edge-triggered flip-flop with clear (3–State)

74AC/ACT11874

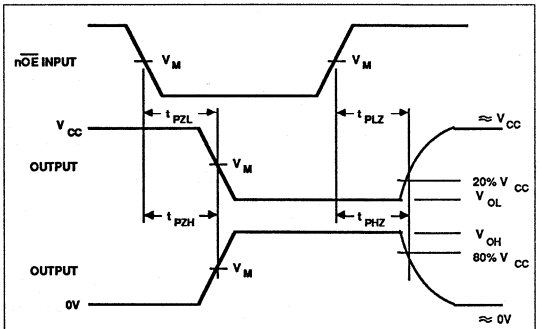
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11874					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	125	140		125		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQ_n	1	3.7 4.1	6.6 7.8	8.4 9.5	3.7 4.1	9.4 10.6	ns
t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n	4	3.5	7.8	10.5	3.5	11.8	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	2	1.6 2.4	4.6 6.0	6.7 8.6	1.6 2.4	7.4 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	2	5.4 4.9	7.4 7.1	8.9 8.5	5.4 4.9	9.4 9.1	ns
t_W	Clock pulse width High or Low	1	4.0			4.0		ns
t_W	$n\overline{MR}$ pulse width Low	4	4.0			4.0		ns
t_S	Setup time nD_n to nCP	3	5.0			5.0		ns
t_H	Hold time nD_n to nCP	3	1.0			1.0		ns
t_{rec}	Recovery time $n\overline{MR}$ to nCP	4	2.0			2.0		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing the Clock Input (nCP) to Output (nQ_n) Propagation Delays and Clock Input (nCP) Pulse Width

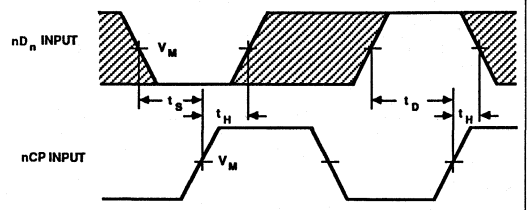


Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

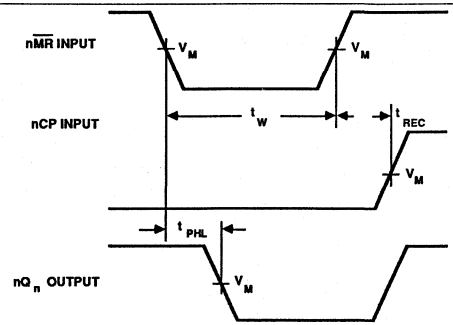
Dual 4-bit D-type edge-triggered flip-flop with clear (3–State)

74AC/ACT11874

WAVEFORMS (continued)



Waveform 3. Waveforms Showing the Data Set-up and Hold Times for nD$_n$ Input to nCP Input

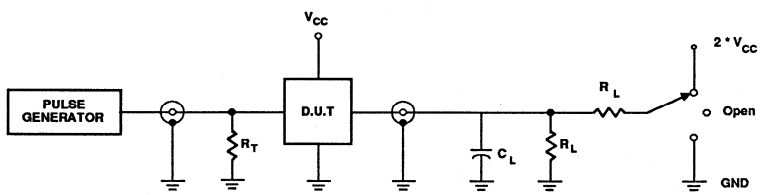


Waveform 4. Waveforms Showing Master Reset (nMR) Pulse Width, Master Reset to Output Delay and Master Reset to Clock (nCP) Recovery Time

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11898

10-bit serial-in parallel-out shift register

FEATURES

- Gated serial data inputs
- Fully buffered clock and data inputs
- Fully synchronous data transfers
- Typical shift frequency of 100MHz
- Asynchronous master reset
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11898 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11898 10-bit Serial-In Parallel-Out Shift Register is an edge-triggered shift register with serial data entry and an output from each of the 10 stages. Data is entered serially through one of two inputs (A • B); either input

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/ t_{PHL}	Propagation delay CP to Q_n ($\overline{MR}$ = High)	C_L = 50pF	5.9	6.9	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	122	117	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	100	100	MHz

Note:

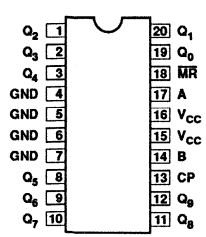
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

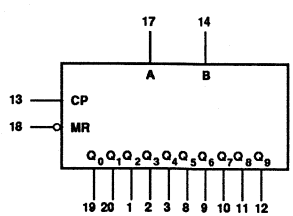
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11898N 74ACT11898N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11898D 74ACT11898D

PIN CONFIGURATION

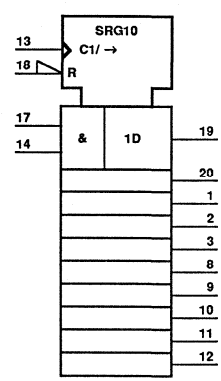
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



10-bit serial-in parallel-out shift register | 74AC/ACT11898

can be used as an active-High enable for data entry through the other input. Otherwise both inputs must be connected to the input data or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input and enters the logical AND of the two inputs (A • B) that existed one setup time before the rising clock edge into Q_0. A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

PIN DESCRIPTION

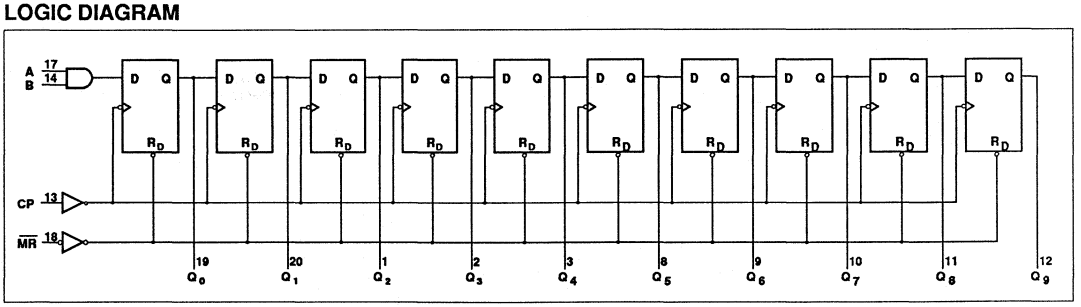
PIN NUMBER	SYMBOL	NAME AND FUNCTION
18	$\overline{MR}$	Asynchronous master reset (active Low)
13	CP	Clock input (Low-to-High, edge-triggered)
17, 14	A, B	Data inputs
19, 20, 1, 2, 3, 8, 9, 10, 11, 12	Q_0 - Q_9	Parallel outputs outputs
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	$\overline{MR}$	CP	A	B	Q_0	Q_1	—	Q_9
Reset (clear)	L	X	X	X	L	L	—	L
Shift	H	↑	l	l	L	q_0	—	q_9
	H	↑	l	h	L	q_0	—	q_9
	H	↑	h	l	L	q_0	—	q_9
	H	↑	h	h	H	q_0	—	q_9

H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q_n = State of the referenced input (or output) one setup time prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11898			74ACT11898			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±250	mA
	DC ground current		±250	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11898				74ACT11898				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11898					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	40	65		40		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	3.3 3.9	8.1 8.8	9.8 10.5	3.3 3.9	10.8 11.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	4.1	9.3	11.2	4.1	12.3	ns
t_S	Setup time, High or Low A, B to CP	3	14.0			14.0		ns
t_H	Hold time, High or Low A, B to CP	3	0.0			0.0		ns
t_W	Clock pulse width (shift) High or Low	1	12.5			12.5		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.5			1.5		ns

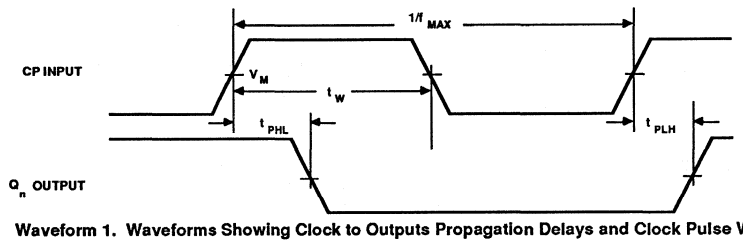
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11898					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	75	100		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	2.7 3.1	5.5 6.3	7.4 8.3	2.7 3.1	8.1 9.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	3.8	6.7	8.6	3.8	9.4	ns
t_S	Setup time, High or Low A, B to CP	3	8.5			8.5		ns
t_H	Hold time, High or Low A, B to CP	3	0.0			0.0		ns
t_W	Clock pulse width (shift) High or Low	1	6.7			6.7		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.0			4.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.5			1.5		ns

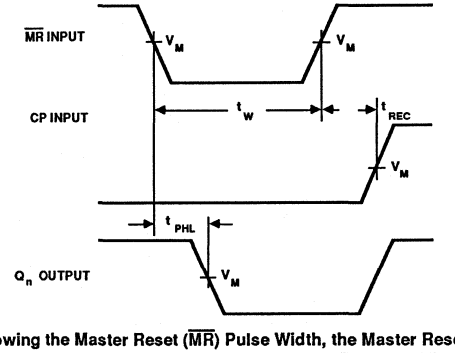
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11898					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	75	100		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	1	4.1 4.4	6.5 7.2	8.0 8.8	4.1 4.4	8.8 9.6	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	4.6	8.0	10.3	4.6	11.3	ns
t_S	Setup time, High or Low A, B to CP	3	9.5			9.5		ns
t_H	Hold time, High or Low A, B to CP	3	0.0			0.0		ns
t_W	Clock pulse width (shift) High or Low	1	6.7			6.7		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	1.5			1.5		ns

AC WAVEFORMS

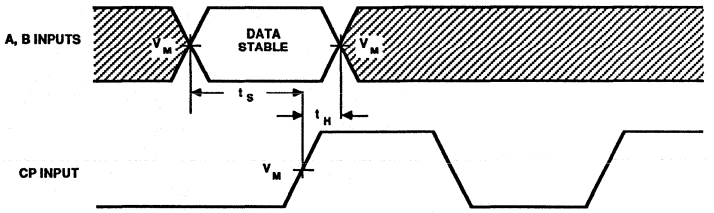


Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Master Reset ($\overline{MR}$) Pulse Width, the Master Reset to Output (Q_n) Propagation Delays, and the Master Reset to Clock (CP) Recovery Time

AC WAVEFORMS (Continued)

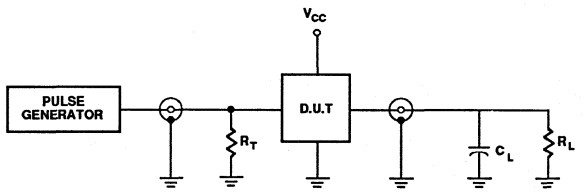


Waveform 3. Waveforms Showing the Data Set-up and Hold Times for the InputS (A,B)

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

AC11979: Preliminary Specification
ACT11979: Product Specification
8-bit multiplexed I/O read-back register

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11979 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11979 device is an 8-bit multiplexed I/O read-back register. When the Output Enable ($\overline{OE}$) input is held High, it loads data on the rising edge of the Clock (CP). When the Clock is held High or Low, the data is held in the registers. When the Output Enable is Low, the data held in the register is visible on the I/O pins (I/O_n).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PZH}/ t_{PZL}	Propagation delay $\overline{OE}$ to I/O_n	C_L = 50pF	6.2	6.2	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; Disabled	12	15	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
$C_{I/O}$	I/O capacitance	$V_{I/O}$ = 0V or V_{CC}; Disabled	8.5	8.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

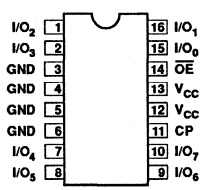
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

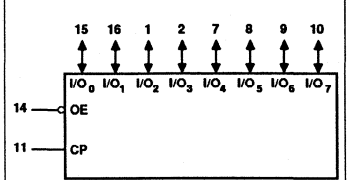
PACKAGES	TEMPERATURE RANGE	ORDER CODE
16-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11979N 74ACT11979N
16-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11979D 74ACT11979D

PIN CONFIGURATION

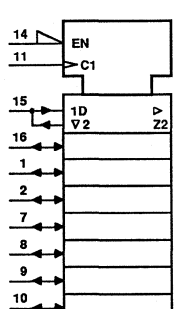
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



8-bit multiplexed I/O read-back register 74AC/ACT11979

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
14	$\overline{OE}$	Output enable input (active Low)
11	CP	Clock input
15, 16, 1, 2 7, 8, 9, 10	I/O_0 - I/O_7	Data inputs/outputs (3-state)
3, 4, 5, 6	GND	Ground (0V)
12, 13	V_{CC}	Positive supply voltage

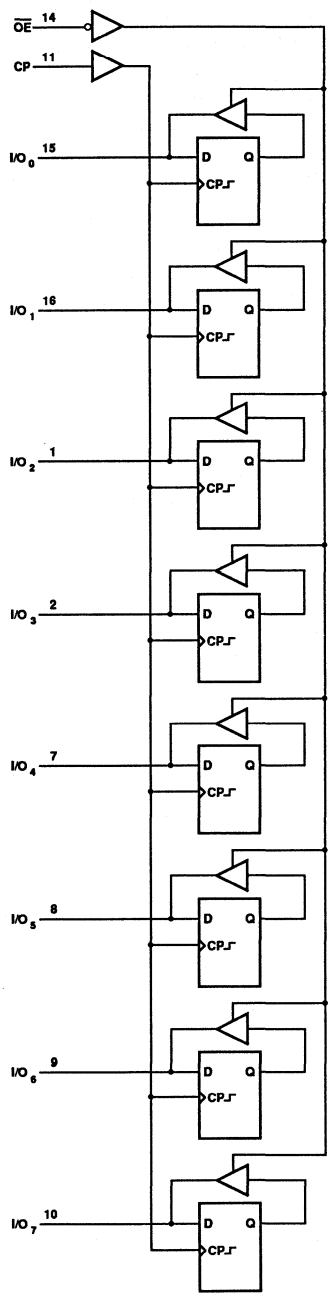
FUNCTION TABLE

$\overline{OE}$	CP	I/O_n	OPERATION
L	X*	Data out	Output data
H	↑	l h	Load data
H	H L	Z	Hold data

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low volatge level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
Z = High-impedance (OFF) state
* The register is loaded on any Low-to-High transition

8-bit multiplexed I/O read-back register 74AC/ACT11979

LOGIC DIAGRAM



8-bit multiplexed I/O read-back register 74AC/ACT11979

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11979			74ACT11979			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8-bit multiplexed I/O read-back register 74AC/ACT11979

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11979				74ACT11979				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{OZ}	3-State output off-state current	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND		5.5		±0.5		5.0		±0.5		5.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

8-bit multiplexed I/O read-back register 74AC/ACT11979

AC ELECTRICAL CHARACTERISTICS AT 3.0V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11979					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PZH} t_{PZL}	Output enable time to High and Low level	1	3.6 5.0	7.9 9.2	9.9 11.1	3.6 5.0	10.9 12.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	1	4.1 3.7	7.2 6.6	8.7 8.2	4.1 3.7	9.1 8.5	ns
t_W	CP pulse width High or Low	2	4.0			4.0		ns
t_S	Setup time I/O_n to CP	2	6.0			6.0		ns
t_H	Hold time CP to I/O_n	2	0.0			0.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

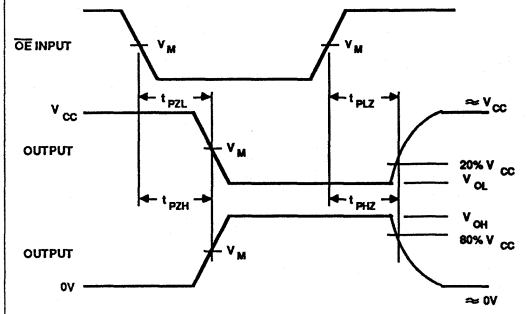
SYMBOL	PARAMETER	WAVEFORM	74AC11979					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PZH} t_{PZL}	Output enable time to High and Low level	1	3.1 4.4	5.4 7.0	7.3 9.2	3.1 4.4	7.9 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	1	3.8 3.4	5.8 5.5	7.8 7.5	3.8 3.4	8.2 7.8	ns
t_W	CP pulse width High or Low	2	3.0			3.0		ns
t_S	Setup time I/O_n to CP	2	5.0			5.0		ns
t_H	Hold time CP to I/O_n	2	0.5			0.5		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

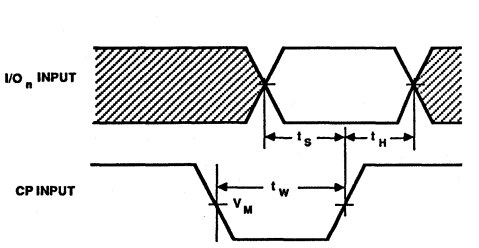
SYMBOL	PARAMETER	WAVEFORM	74ACT11979					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PZH} t_{PZL}	Output enable time to High and Low level	1	2.4 3.0	5.8 7.5	9.1 11.3	2.4 3.0	9.9 12.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	1	4.5 4.2	6.8 6.7	9.4 9.3	4.5 4.2	10.0 9.8	ns
t_W	CP pulse width High or Low	2	4.0			4.0		ns
t_S	Setup time I/O_n to CP	2	4.5			4.5		ns
t_H	Hold time CP to I/O_n	2	1.5			1.5		ns

8-bit multiplexed I/O read-back register 74AC/ACT11979

AC WAVEFORMS



Waveform 1. Waveforms Showing the 3-State Output Enable and Disable Times

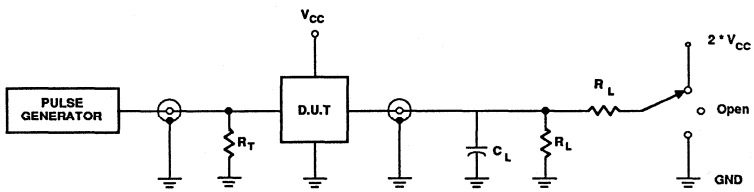


Waveform 2. Waveforms Showing the Data Setup and Hold Times for I/O_n Input to CP Input

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2*V_{CC}
t_{PHZ}/t_{PZH}	GND

SWITCH POSITION

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

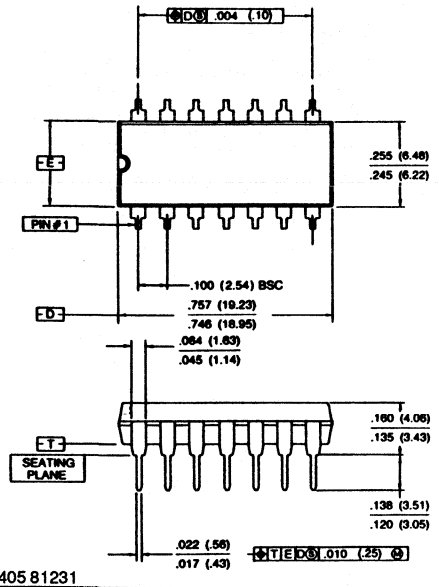
$t_r = t_f$ = 3ns

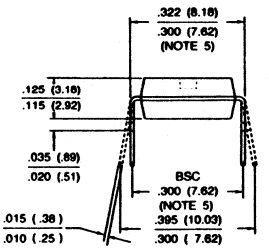
Section 4
Packaging Information

ACL Supplement

Packaging Information

14-PIN PLASTIC DUAL-IN-LINE PACKAGE



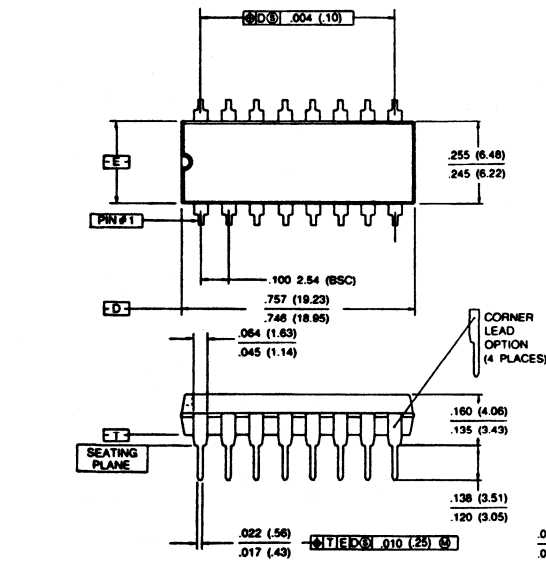


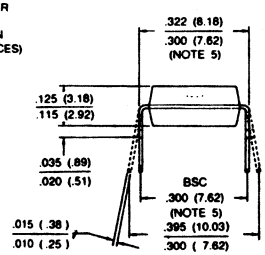
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

853-0405 81231

NH1

16-PIN PLASTIC DUAL-IN-LINE PACKAGE





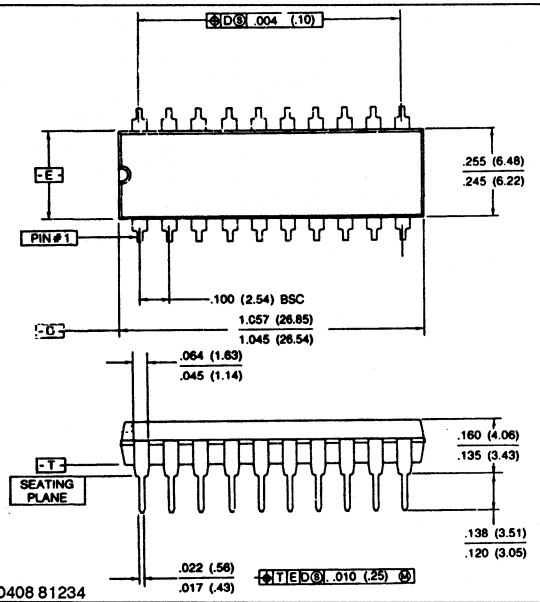
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0406 81232

NJ1

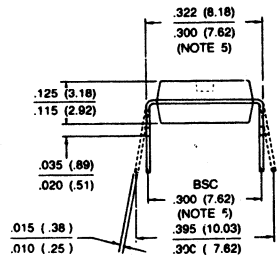
Packaging Information

20-PIN PLASTIC DUAL-IN-LINE PACKAGE

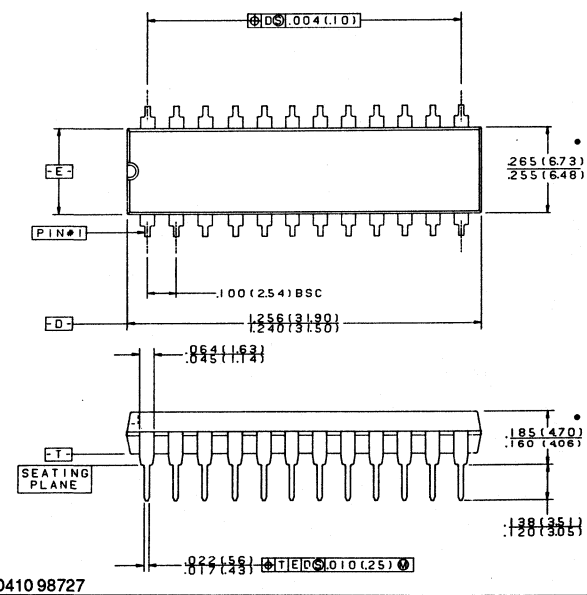


NOTES:

1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

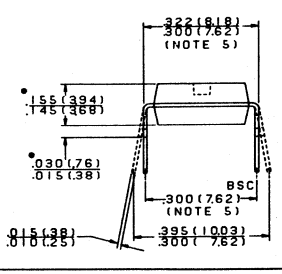


24-PIN PLASTIC DUAL-IN-LINE PACKAGE



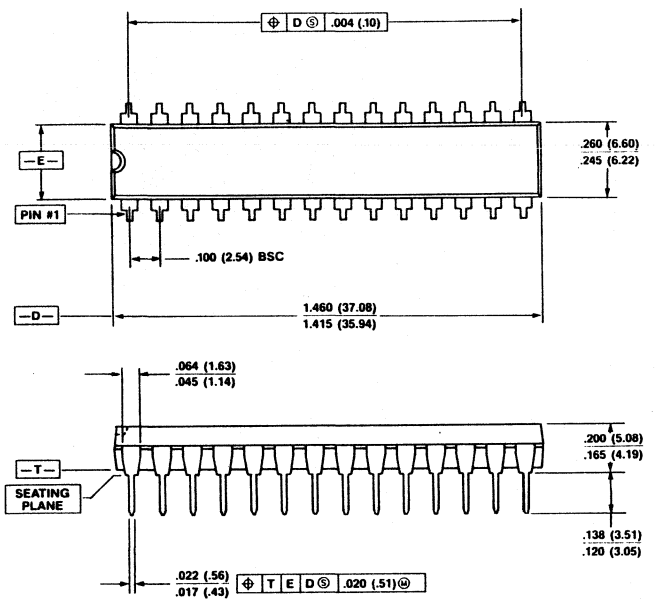
NOTES

1. CONTROLLING DIMENSION: INCHES METRIC ARE SHOWN IN PARENTHESES.
2. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-001-AF FOR STANDARD DUAL IN-LINE (DIP) PACKAGE .300 INCH ROW SPACING (PLASTIC) 24 LEADS (ISSUE B. 7/85)
3. DIMENSION AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T" "D" AND "E" ARE REFERENCE DATEMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (.25MM) ON ANY SIDE.
5. THESE DIMENSIONS MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#24 WHEN VIEWED FROM THE TOP.



Packaging Information

28-PIN PLASTIC DUAL-IN-LINE PACKAGE



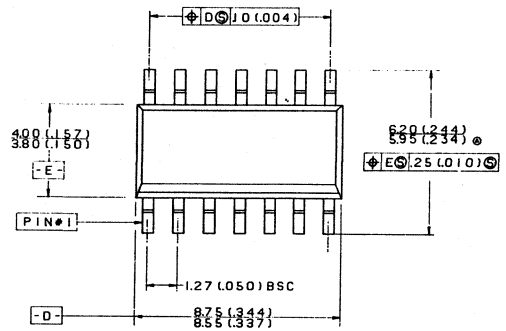
NOTES:

1. Controlling dimensions: inches. Metric are shown in parentheses.
2. Dimensions are tolerancing per ANSI Y14.5M-1982.
3. "T", "D", and "E" are reference datums on the molded body and do not include mold-flash or protrusions which shall not exceed .010 inch (.25 mm) on any side.
4. These dimensions measured with the leads constrained to be perpendicular to plane "T".
5. Pin numbers start with #1 and continue counterclockwise to pin #28 when viewed from the top.

853-0864 89398 NQ1

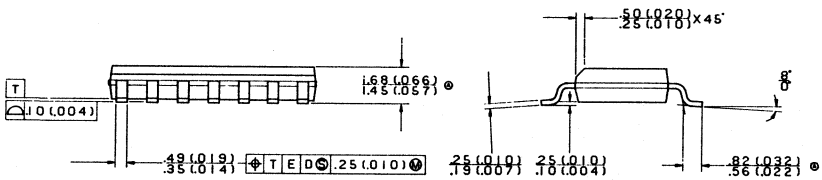
Packaging Information

14-PIN PLASTIC PLASTIC SO PACKAGE



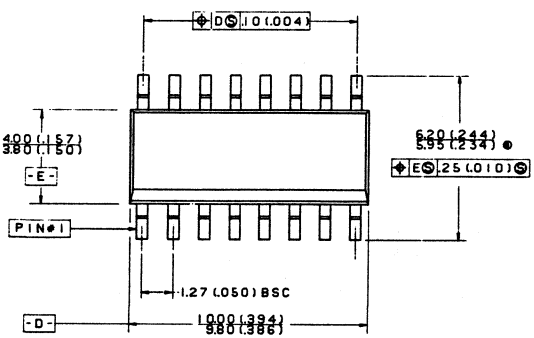
NOTES

1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-012-AB FOR STANDARD SMALL OUTLINE (SO) PACKAGE, 14 LEADS, 3.75MM (.150") BODY WIDTH (ISSUE A. JUNE 1985).
2. CONTROLLING DIMENSIONS ARE MM. INCH DIMENSIONS IN PARENTHESES.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T", "D" AND "E" ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15MM (.006") ON ANY SIDE.
5. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#14 WHEN VIEWEN FROM TOP.
6. SIGNETICS ORDERING CODE FOR A PRODUCT PACKAGED IN A PLASTIC SMALL OUTLINE (SO) PACKAGE IS THE SUFFIX D AFTER THE PRODUCT NUMBER.



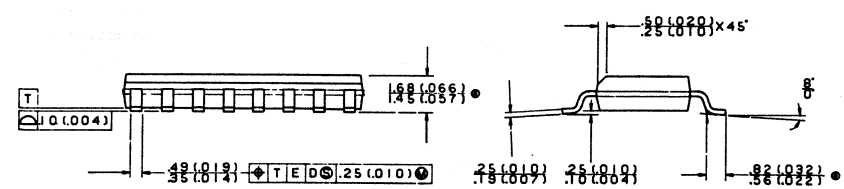
853-0175 91504 DH1

16-PIN PLASTIC PLASTIC SO PACKAGE



NOTES

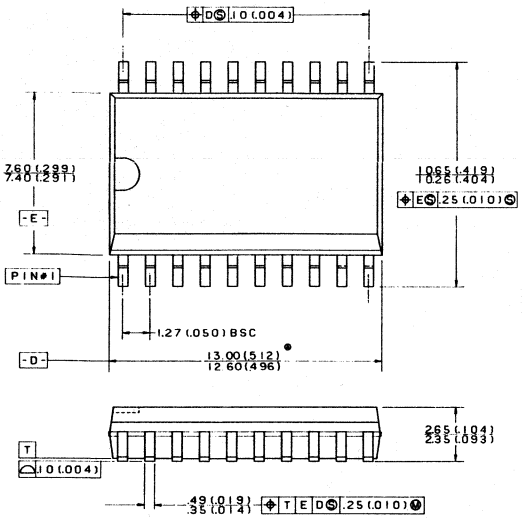
1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-012-AC FOR STANDARD SMALL OUTLINE (SO) PACKAGE, 16 LEADS, 3.75MM (.150") BODY WIDTH (ISSUE A. JUNE 1985).
2. CONTROLLING DIMENSIONS ARE MM. INCH DIMENSIONS IN PARENTHESES.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T", "D" AND "E" ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15MM (.006") ON ANY SIDE.
5. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#16 WHEN VIEWED FROM TOP.
6. SIGNETICS ORDERING CODE FOR A PRODUCT PACKAGED IN A PLASTIC SMALL OUTLINE (SO) PACKAGE IS THE SUFFIX D AFTER THE PRODUCT NUMBER.



853-0005 91504 DJ1

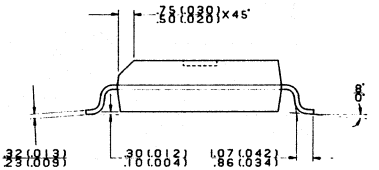
Packaging Information

20-PIN PLASTIC PLASTIC SO PACKAGE



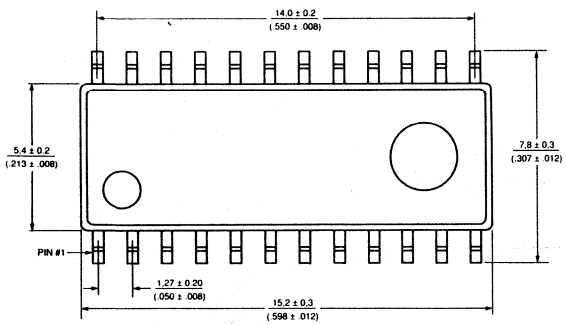
NOTES

1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-013-AC FOR STANDARD SMALL OUTLINE (SO) PACKAGE 20 LEADS 7.50MM (.300") BODY WIDTH (ISSUE A. JUNE 1985).
2. CONTROLLING DIMENSIONS ARE MM. INCH DIMENSIONS IN PARENTHESES.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T", "D" AND "E" ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15MM (.006") ON ANY SIDE.
5. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#20 WHEN VIEWED FROM TOP.
6. SIGNETICS ORDERING CODE FOR A PRODUCT PACKAGED IN A PLASTIC SMALL OUTLINE (SO) PACKAGE IS THE SUFFIX D AFTER THE PRODUCT NUMBER.



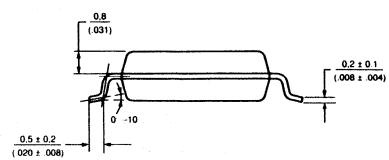
853-0172 82948 DL1

24-PIN PLASTIC PLASTIC SO PACKAGE



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm) DIMENSIONS IN PARENTHESES ARE IN INCHES.
2. PIN NUMBERS START WITH PIN #1 AND CONTINUE COUNTERCLOCKWISE TO PIN #24 WHEN VIEWED FROM TOP.

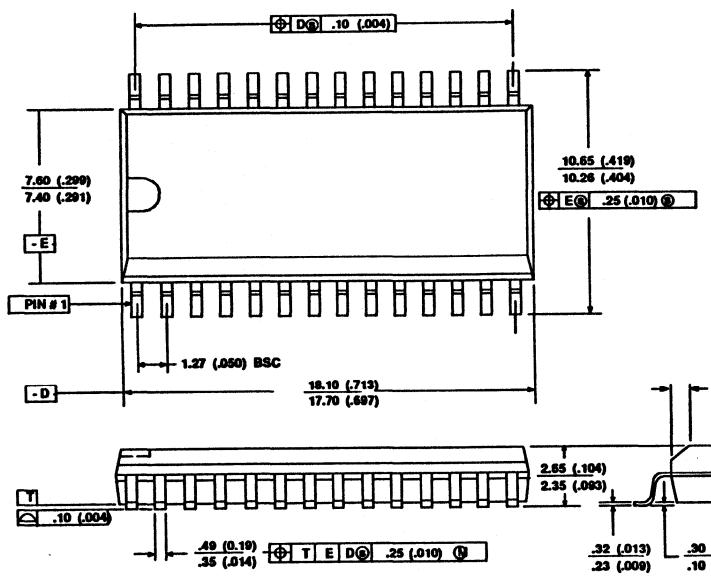


* THIS IS NOT A JEDEC OUTLINE FOR JEDEC SO 24 OUTLINE SEE DRAWING 853-0173

853-1460 000238 EIAJ Type II Outline DNB

Packaging Information

28-PIN PLASTIC PLASTIC SO PACKAGE



NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #28 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

853-0006 81217 DQ2

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of seven series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MAGNETIC PRODUCTS*

LIQUID CRYSTAL DISPLAYS

The contents of each series are listed on pages III to IX.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where application is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

INTEGRATED CIRCUITS

This series of handbooks comprises:

code	handbook title
IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom;** Subscriber sets, Cordless Telephones, Mobile/Cellular, Radio Pagers
IC04	**HE4000B logic family** CMOS
IC05	**Advanced Low-power Schottky (ALS) Logic Series**
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
Supplement to IC07	**Advanced CMOS logic (ACL)**
IC08	**10/100K ECL Logic/Memory/PLD**
IC09	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
IC12	**I^2C-bus compatible ICs**
IC13	**Semi-custom** Programmable Logic Devices (PLD)
IC14	**Microcontrollers** NMOS, CMOS
IC15	**FAST TTL logic series**
Supplement to IC15	**FAST TTL logic series**
IC16	**CMOS integrated circuits for clocks and watches**
IC17	**ICs for Telecom;** ISDN
IC18	**Microprocessors and peripherals**
IC19	**Data communication products**
IC20	**8051-based 16-bit microcontrollers**
IC23	**Advanced BiCMOS interface logic**

DISCRETE SEMICONDUCTORS

This series of data handbooks comprises:

current code	new code	handbook title
S1	**SC01**	**Diodes** High-voltage tripler units
S2a	**SC02**	**Power diodes**
S2b	**SC03**	**Thyristors and triacs**
S3	**SC04**	**Small-signal transistors**
S4a	**SC05**	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07**	**Small-signal field-effect transistors**
S6	**SC08a***	**RF power bipolar transistors**
	SC08b**	**RF power MOS transistors**
	SC09	**RF power modules**
S7	**SC10**	**Surface mounted semiconductors**
S8b	**SC12**	**Optocouplers**
S9	**SC13***	**Power MOS transistors**
S10	**SC14**	**Wideband transistors and wideband hybrid IC modules**
S11	**SC15**	**Microwave transistors**
S15**	**SC16**	**Laser diodes**
S13	**SC17**	**Semiconductor sensors**

* Not yet issued with the new code in this series of handbooks.
** New handbook in this series; will be issued shortly.

PASSIVE COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
C14	**PA01**	**Electrolytic capacitors; solid and non-solid**
C11	**PA02**	**Varistors, thermistors and sensors**
C12	**PA03**	**Potentiometers and switches**
C7	**PA04**	**Variable capacitors**
C22	**PA05***	**Film capacitors**
C15	**PA06**	**Ceramic capacitors**
C9	**PA07***	**Piezoelectric quartz devices**
C13	**PA08**	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

DISPLAY COMPONENTS

This series of data handbooks comprises:

code	handbook title
DC01	**Colour display components** Colour TV Picture Tubes and Assemblies Colour Monitor Tube Assemblies
DC02	**Monochrome monitor tubes and deflection units**
DC03	**Television tuners, coaxial aerial input assemblies**
DC04	**Loudspeakers**
DC05	**Flyback transformers, mains transformers and general-purpose FXC assemblies**

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T3	**PC01**	**High-power klystrons and accessories**
T5	**PC02***	**Cathode-ray tubes**
T6	**PC03***	**Geiger-Müller tubes**
T9	**PC04**	**Photo multipliers**
T10	**PC05**	**Plumbicon camera tubes and accessories**
T11	**PC06**	**Circulators and Isolators**
T12	**PC07**	**Vidicon and Newvicon camera tubes and deflection units**
T13	**PC08**	**Image intensifiers**
T15	**PC09**	**Dry-reed switches**
	PC11	**Solid state image sensors and peripherals integrated circuits**
T9	**PC12***	**Electron multipliers**

* Not yet issued with the new code in this series of handbooks.

MAGNETIC PRODUCTS

This series of data handbooks comprises:

current code	new code	handbook title
C4, C5	MA01	**Soft Ferrites**
C16	MA02*	**Permanent magnet materials**
C19	MA03*	**Piezoelectric ceramics**

* Not yet issued with the new code in this series of handbooks.

LIQUID CRYSTAL DISPLAYS

current code	new code	handbook title
S14	**LCD01**	**Liquid Crystal Displays and driver ICs for LCDs**

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Printed in The Netherlands

9398 178 30011

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